



Q67/ Q65/ H67/ H61 H2-AD

Rev : 1.0

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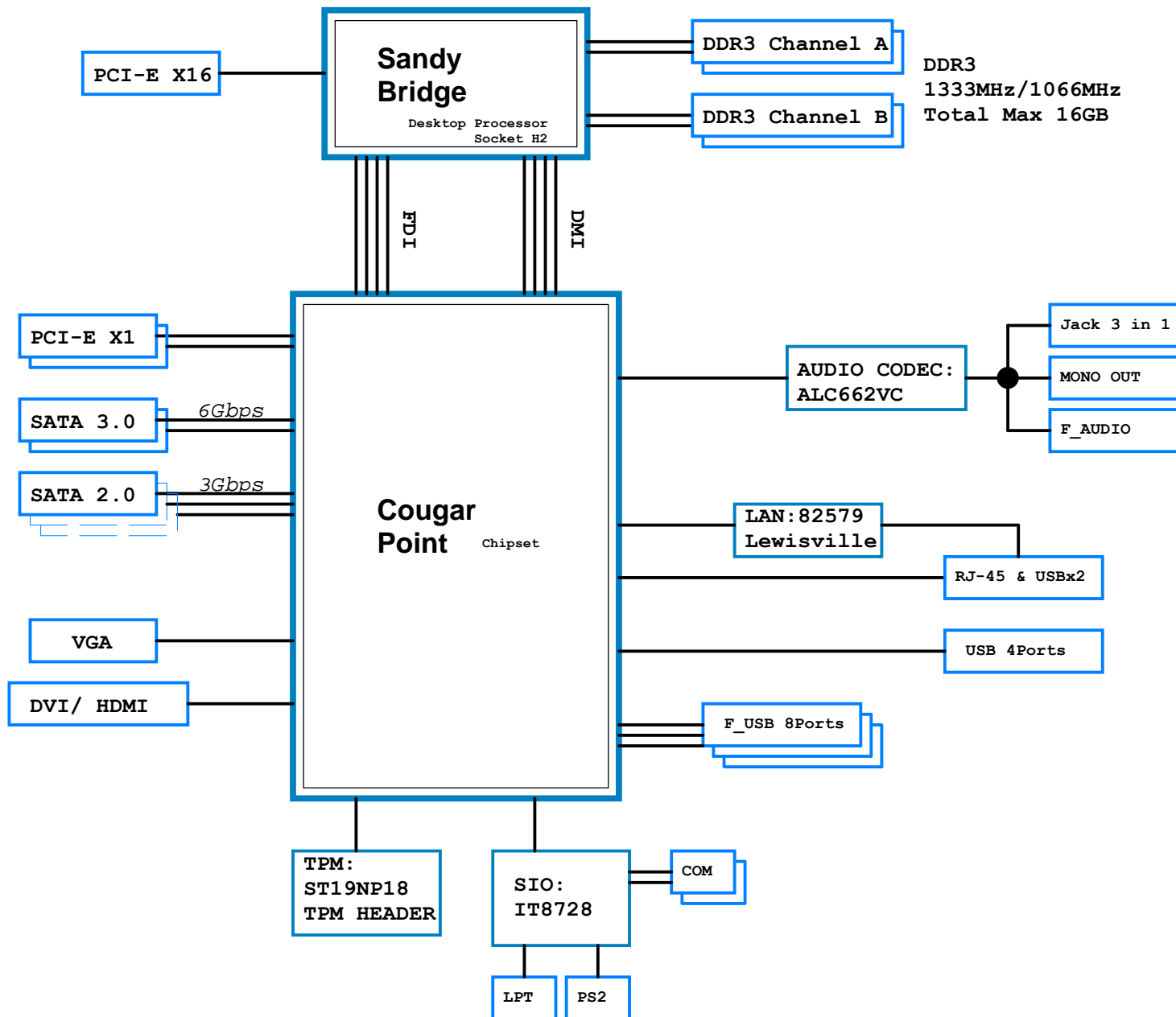
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REVISION HISTORY:

Rev	Date	Notes
V.A	2010/07/22	Initial version
V.B	2010/08/24	
V.C	2010/09/10	
V.1.0	2010/09/16	

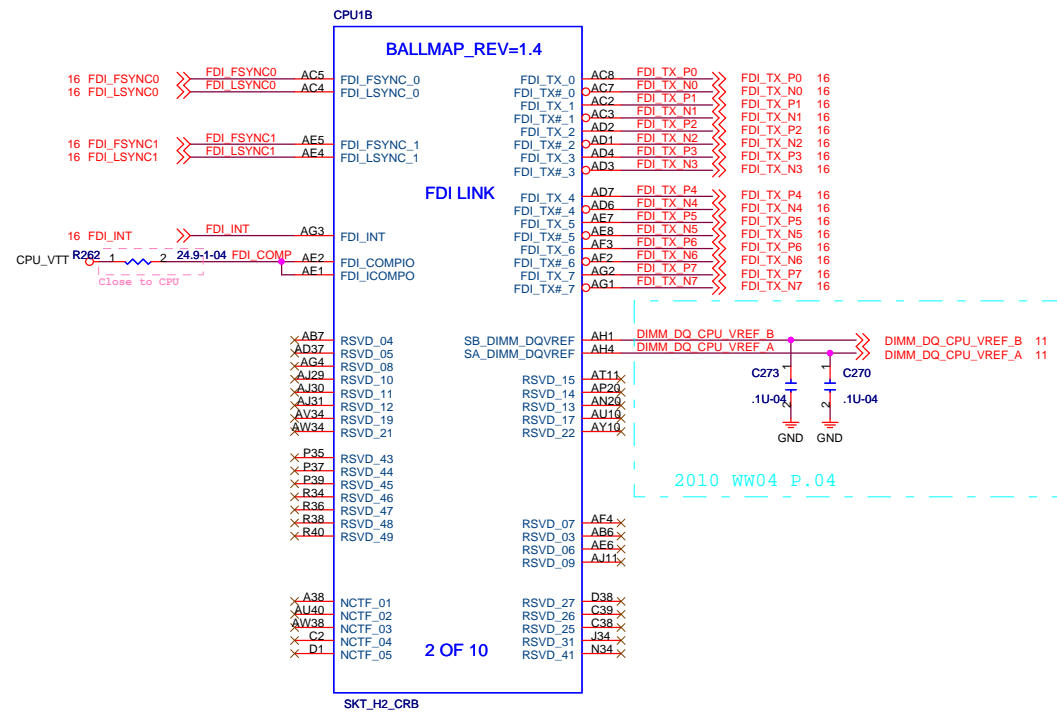
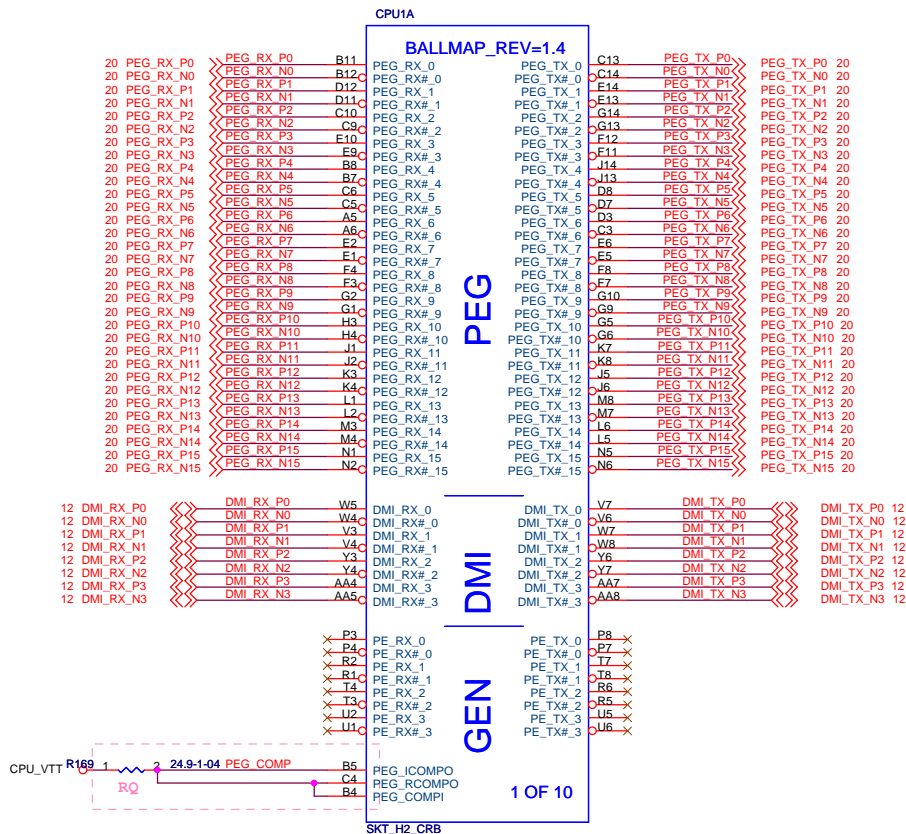


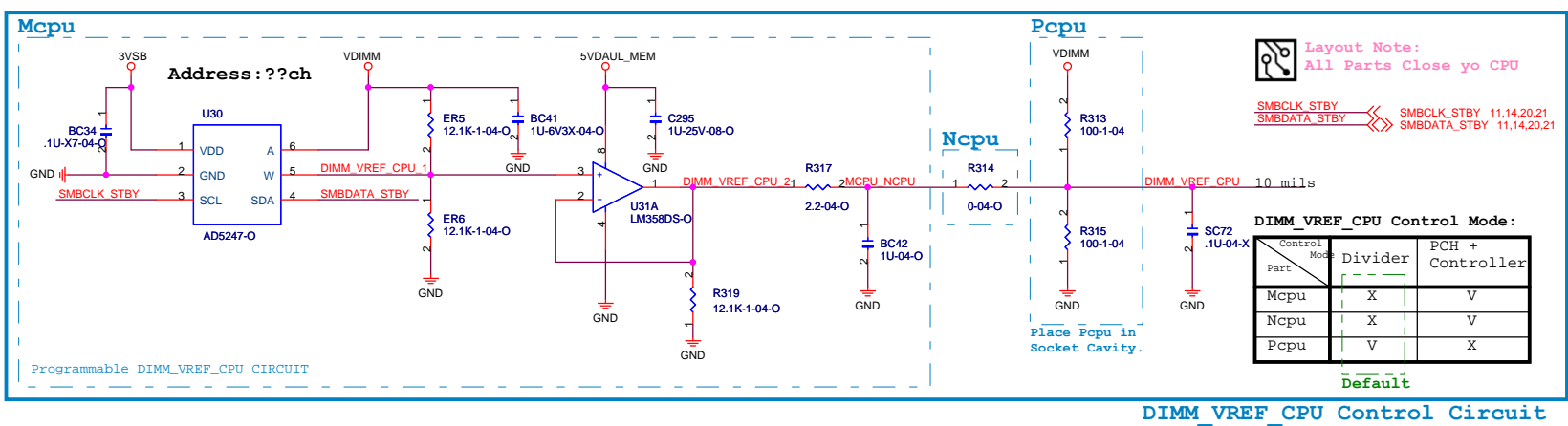
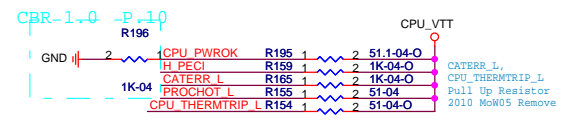
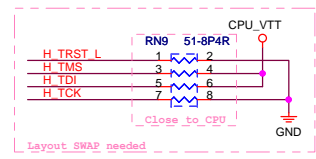
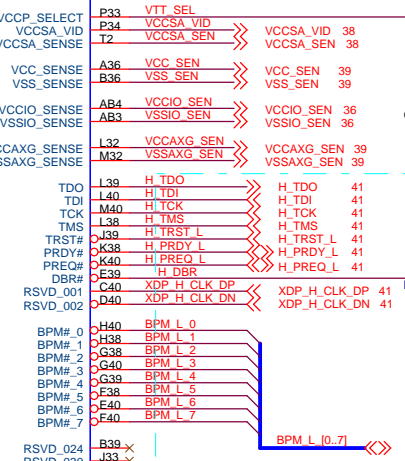
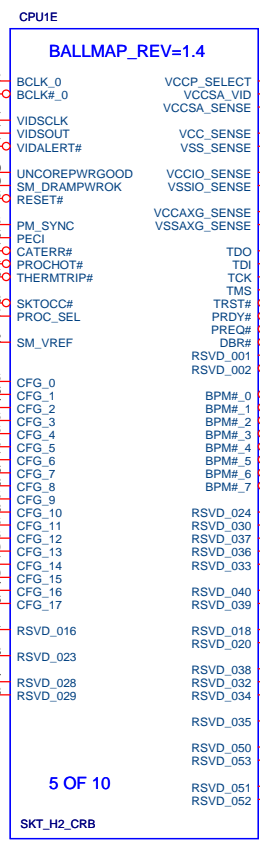
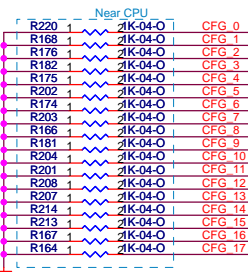
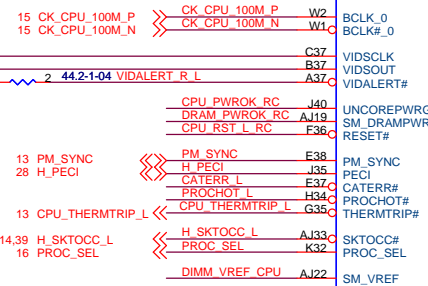
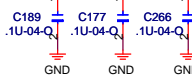
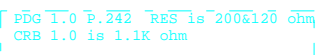
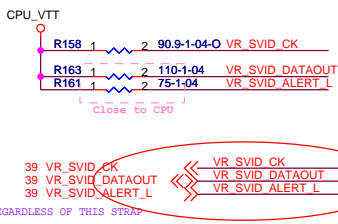
PCH-GPIO function

Pin Name	Power Well	Usage	Default Status
GPIO71	VCC3	LPT Detect	GPI
GPIO22	VCC3	CLR_CMOS	GPI
GPIO38	VCC3	KM Detect	GPI
GPIO39	VCC3	SENSE_Header	GPI
GPIO48	VCC3	SENSE_Header	GPI
GPIO21	VCC3	COM2 Detect	GPI
GPIO36	VCC3	TCM,TPM Detect	GPI
GPIO37	VCC3	TCM,TPM Detect	GPI
GPIO16	VCC3	Reserve for TPM	GPI
GPIO49	VCC3	Reserve for TPM	GPI
GPIO0	VCC3	F_AUDIO Detect	GPI
GPIO33	VCC3	ME Enable/Disable	GPO
GPIO34	VCC3	pull-up	GPI
GPIO13	3VSB	PME	GPI
GPIO24	3VSB	SKTOCC	GPO
GPIO57	3VSB	Board ID(CRB_0.7)	GPI
GPIO61	3VSB	TPM_LPCPD	GPI

SIO-GPIO function

Pin Name	Power Well	Usage	Default Status
GP16		BEEP	
GP23		Power LED	
GP22		Power LED	
Pin Name		Usage	
Pin Name		Usage	
Pin Name		Usage	
Pin Name		Usage	





CFG	H	L	DESCRIPTION
0	reserved	reserved	reserved
1	reserved	reserved	reserved
2	NORMAL	REVERSE	PEGLANE REVERSAL[0], X16
3	reserved	reserved	reserved
4	reserved	*	reserved
5	*	*	PEOFGSEL[0]
6	*	*	PEOFGSEL[1]
7	reserved	reserved	reserved
8	reserved	reserved	reserved
9	reserved	reserved	reserved
10	reserved	reserved	reserved
11	reserved	reserved	reserved
12	reserved	reserved	reserved
13	reserved	reserved	reserved
14	reserved	reserved	reserved
15	reserved	reserved	reserved

CFG_[0..17] HAVE INTERNAL PULL-UPS

PCIE CONFIG	SEL0	SEL1
1 X 16	1	1
2 X 8	0	1

CFG[5:6]:
11=DEFAULT X16,
01=2X8,
10=RESERVED,
00=X8.X4.X4

DIMM_VREF_CPU Control Mode:

Control Mode Part	Divider	PCH + Controller
Mcpu	X	V
Ncpu	X	V
Pcpu	V	X

Default

9 M_DATA_A[0..63]	← M_DATA A[0..63]
9 M_DQS_A_P[0..7]	← M_DQS A P[0..7]
9 M_DQS_A_N[0..7]	← M_DQS A N[0..7]
9 M_MA_A[0..15]	← M_MA A[0..15]
9 M_BS_A[0..2]	← M_BS A[0..2]
9 M_CS_A_L[0..3]	← M_CS A_L[0..3]
9 M_CKE_A[0..3]	← M_CKE A[0..3]
9 M_ODT_A[0..3]	← M_ODT A[0..3]
9 M_CLK_A_P[0..3]	← M_CLK A_P[0..3]
9 M_CLK_A_N[0..3]	← M_CLK A_N[0..3]
9 M_WE_A_L	← M_WE A_L
9 M_CAS_A_L	← M_CAS A_L
9 M_RAS_A_L	← M_RAS A_L

DDR3 CH.A

9,10 DDR3_DRAMRST_L ← DDR3_DRAMRST_L

10 M_DATA_B[0..63]	← M_DATA B[0..63]
10 M_DQS_B_P[0..7]	← M_DQS B P[0..7]
10 M_DQS_B_N[0..7]	← M_DQS B N[0..7]
10 M_MA_B[0..15]	← M_MA B[0..15]
10 M_BS_B[0..2]	← M_BS B[0..2]
10 M_CS_B_L[0..3]	← M_CS B_L[0..3]
10 M_CKE_B[0..3]	← M_CKE B[0..3]
10 M_ODT_B[0..3]	← M_ODT B[0..3]
10 M_CLK_B_P[0..3]	← M_CLK B_P[0..3]
10 M_CLK_B_N[0..3]	← M_CLK B_N[0..3]
10 M_WE_B_L	← M_WE B_L
10 M_CAS_B_L	← M_CAS B_L
10 M_RAS_B_L	← M_RAS B_L

DDR3 CH.B

M_DATA_A0	AJ3	SA_DQ_0
M_DATA_A1	AJ4	SA_DQ_1
M_DATA_A2	AL3	SA_DQ_2
M_DATA_A3	AL4	SA_DQ_3
M_DATA_A4	AJ2	SA_MA_4
M_DATA_A5	AJ1	SA_DQ_5
M_DATA_A6	AL1	SA_DQ_6
M_DATA_A7	AL2	SA_DQ_7
M_DATA_A8	AN1	SA_MA_8
M_DATA_A9	AN4	SA_DQ_9
M_DATA_A10	AR3	SA_DQ_10
M_DATA_A11	AR4	SA_DQ_11
M_DATA_A12	AN2	SA_DQ_12
M_DATA_A13	AR2	SA_DQ_13
M_DATA_A14	AR1	SA_DQ_14
M_DATA_A15	AV2	SA_DQ_15
M_DATA_A16	AV3	SA_DQ_16
M_DATA_A17	AV5	SA_DQ_17
M_DATA_A18	AU2	SA_DQ_18
M_DATA_A19	AU3	SA_DQ_19
M_DATA_A20	AU4	SA_DQ_20
M_DATA_A21	AU5	SA_DQ_21
M_DATA_A22	AY5	SA_DQ_22
M_DATA_A23	AY6	SA_DQ_23
M_DATA_A24	AU7	SA_DQ_24
M_DATA_A25	AV7	SA_DQ_25
M_DATA_A26	AV9	SA_DQ_26
M_DATA_A27	AU8	SA_DQ_27
M_DATA_A28	AV7	SA_DQ_28
M_DATA_A29	AW7	SA_DQ_29
M_DATA_A30	AY9	SA_DQ_30
M_DATA_A31	AU35	SA_DQ_31
M_DATA_A32	AW37	SA_DQ_32
M_DATA_A33	AU39	SA_DQ_33
M_DATA_A34	AW35	SA_DQ_34
M_DATA_A35	AY36	SA_DQ_35
M_DATA_A36	AU38	SA_DQ_36
M_DATA_A37	AU37	SA_DQ_37
M_DATA_A38	AR37	SA_DQ_38
M_DATA_A39	AR37	SA_DQ_39
M_DATA_A40	AN37	SA_DQ_40
M_DATA_A41	AN38	SA_DQ_41
M_DATA_A42	AN37	SA_DQ_42
M_DATA_A43	AR39	SA_DQ_43
M_DATA_A44	AR38	SA_DQ_44
M_DATA_A45	AN39	SA_DQ_45
M_DATA_A46	AN40	SA_DQ_46
M_DATA_A47	AL40	SA_DQ_47
M_DATA_A48	AL37	SA_DQ_48
M_DATA_A49	AJ38	SA_DQ_49
M_DATA_A50	AJ37	SA_DQ_50
M_DATA_A51	AL38	SA_DQ_51
M_DATA_A52	AL39	SA_DQ_52
M_DATA_A53	AJ39	SA_DQ_53
M_DATA_A54	AJ40	SA_DQ_54
M_DATA_A55	AG40	SA_DQ_55
M_DATA_A56	AG37	SA_DQ_56
M_DATA_A57	AE38	SA_DQ_57
M_DATA_A58	AE37	SA_DQ_58
M_DATA_A59	AG39	SA_DQ_59
M_DATA_A60	AG38	SA_DQ_60
M_DATA_A61	AE39	SA_DQ_61
M_DATA_A62	AE40	SA_DQ_62
M_DATA_A63	AE40	SA_DQ_63

M_DQS_A_P0	AK3	SA_DQS_0
M_DQS_A_P1	AP3	SA_DQS_1
M_DQS_A_P2	AW4	SA_DQS_2
M_DQS_A_P3	AV8	SA_DQS_3
M_DQS_A_P4	AV37	SA_DQS_4
M_DQS_A_P5	AP38	SA_DQS_5
M_DQS_A_P6	AK38	SA_DQS_6
M_DQS_A_P7	AF38	SA_DQS_7
M_DQS_A_N0	AK2	SA_DQS#_0
M_DQS_A_N1	AP2	SA_DQS#_1
M_DQS_A_N2	AV4	SA_DQS#_2
M_DQS_A_N3	AW8	SA_DQS#_3
M_DQS_A_N4	AV38	SA_DQS#_4
M_DQS_A_N5	AP39	SA_DQS#_5
M_DQS_A_N6	AK39	SA_DQS#_6
M_DQS_A_N7	AF39	SA_DQS#_7

SM_DRAMRST#

SA_DQS_8
SA_DQS#_8

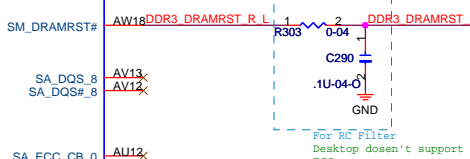
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SA_ECC_CB_6
SA_ECC_CB_7

DDR_0
3 OF 10

SKT_H2_CRB
DDR3 CH.A

DDR3 CH.A

10'06'28 ADD for TRACE Length



Pay Attention to This Part!

M_DATA_B0	AG7	SB_DQ_0
M_DATA_B1	AG8	SB_DQ_1
M_DATA_B2	AJ8	SB_DQ_2
M_DATA_B3	AG5	SB_DQ_3
M_DATA_B4	AG6	SB_DQ_4
M_DATA_B5	AJ6	SB_DQ_5
M_DATA_B6	AL7	SB_DQ_6
M_DATA_B7	AL7	SB_DQ_7
M_DATA_B8	AM7	SB_DQ_8
M_DATA_B9	AM7	SB_DQ_9
M_DATA_B10	AM10	SB_DQ_10
M_DATA_B11	AL10	SB_DQ_11
M_DATA_B12	AL6	SB_DQ_12
M_DATA_B13	AL9	SB_DQ_13
M_DATA_B14	AM9	SB_DQ_14
M_DATA_B15	AP7	SB_DQ_15
M_DATA_B16	AR7	SB_DQ_16
M_DATA_B17	AP10	SB_DQ_17
M_DATA_B18	AR10	SB_DQ_18
M_DATA_B19	AP6	SB_DQ_19
M_DATA_B20	AR6	SB_DQ_20
M_DATA_B21	AP9	SB_DQ_21
M_DATA_B22	AR9	SB_DQ_22
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M_DATA_B24	AM13	SB_DQ_24
M_DATA_B25	AR13	SB_DQ_25
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M_DATA_B31	AL28	SB_DQ_31
M_DATA_B32	AP28	SB_DQ_32
M_DATA_B33	AR29	SB_DQ_33
M_DATA_B34	AL29	SB_DQ_34
M_DATA_B35	AP28	SB_DQ_35
M_DATA_B36	AR29	SB_DQ_36
M_DATA_B37	AM28	SB_DQ_37
M_DATA_B38	AM29	SB_DQ_38
M_DATA_B39	AP32	SB_DQ_39
M_DATA_B40	AP31	SB_DQ_40
M_DATA_B41	AP35	SB_DQ_41
M_DATA_B42	AP34	SB_DQ_42
M_DATA_B43	AR32	SB_DQ_43
M_DATA_B44	AR31	SB_DQ_44
M_DATA_B45	AR35	SB_DQ_45
M_DATA_B46	AR34	SB_DQ_46
M_DATA_B47	AM32	SB_DQ_47
M_DATA_B48	AM31	SB_DQ_48
M_DATA_B49	AL35	SB_DQ_49
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M_DATA_B51	AM34	SB_DQ_51
M_DATA_B52	AL31	SB_DQ_52
M_DATA_B53	AM35	SB_DQ_53
M_DATA_B54	AL34	SB_DQ_54
M_DATA_B55	AH35	SB_DQ_55
M_DATA_B56	AH34	SB_DQ_56
M_DATA_B57	AE34	SB_DQ_57
M_DATA_B58	AE35	SB_DQ_58
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M_DATA_B60	AJ34	SB_DQ_60
M_DATA_B61	AF33	SB_DQ_61
M_DATA_B62	AF35	SB_DQ_62
M_DATA_B63	AF35	SB_DQ_63

M_DQS_B_P0	AH7	SB_DQS_0
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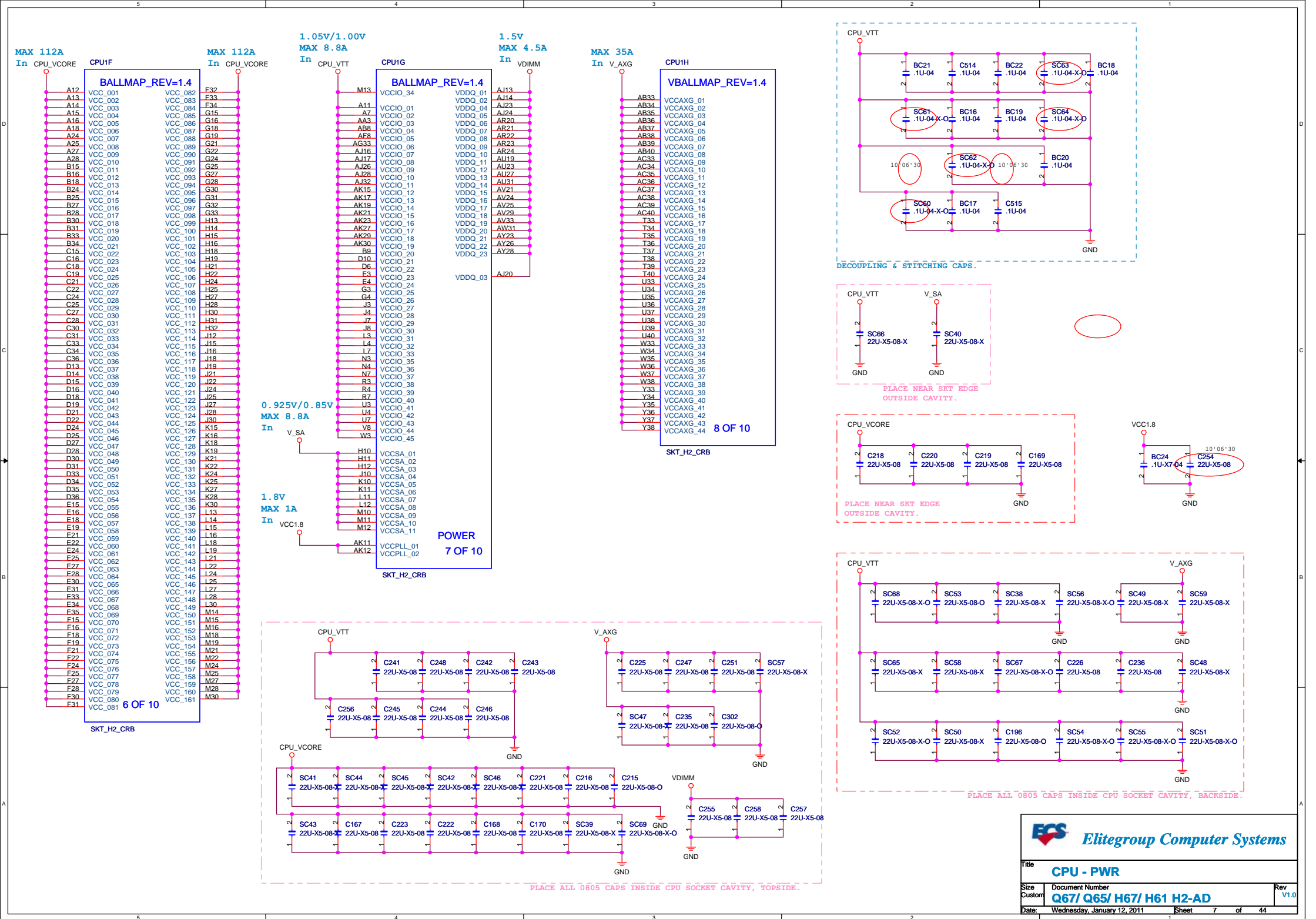
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SB_DQ_4	AP19	M_MA_B4
SB_DQ_5	AP18	M_MA_B5
SB_DQ_6	AM18	M_MA_B6
SB_DQ_7	AL18	M_MA_B7
SB_DQ_8	AN18	M_MA_B8
SB_DQ_9	AY17	M_MA_B9
SB_DQ_10	AN23	M_MA_B10
SB_DQ_11	AU17	M_MA_B11
SB_DQ_12	AT18	M_MA_B12
SB_DQ_13	AR26	M_MA_B13
SB_DQ_14	AY16	M_MA_B14
SB_DQ_15	AV16	M_MA_B15
SB_DQ_16	AR25	M_WE_B_L
SB_DQ_17	AK25	M_CAS_B_L
SB_DQ_18	AP24	M_RAS_B_L
SB_DQ_19	AP23	M_BS_B0
SB_DQ_20	AM24	M_BS_B1
SB_DQ_21	AW17	M_BS_B2
SB_DQ_22	AN25	M_CS_B_L0
SB_DQ_23	AN26	M_CS_B_L1
SB_DQ_24	AT25	M_CS_B_L2
SB_DQ_25	AT26	M_CS_B_L3
SB_DQ_26	AU16	M_CKE_B0
SB_DQ_27	AW15	M_CKE_B2
SB_DQ_28	AV15	M_CKE_B3
SB_DQ_29	AL26	M_ODT_B0
SB_DQ_30	AP26	M_ODT_B2
SB_DQ_31	AK26	M_ODT_B3
SB_DQ_32	AL21	M_CLK_B_P0
SB_DQ_33	AL22	M_CLK_B_N0
SB_DQ_34	AL20	M_CLK_B_P1
SB_DQ_35	AK20	M_CLK_B_N1
SB_DQ_36	AL23	M_CLK_B_P2
SB_DQ_37	AM22	M_CLK_B_N2
SB_DQ_38	AP21	M_CLK_B_P3
SB_DQ_39	AN21	M_CLK_B_N3
SB_DQS_0	AN16	
SB_DQS_1	AN15	
SB_DQS_2		
SB_DQS_3		
SB_DQS_4	AL16	
SB_DQS_5	AM16	
SB_DQS_6	AP16	
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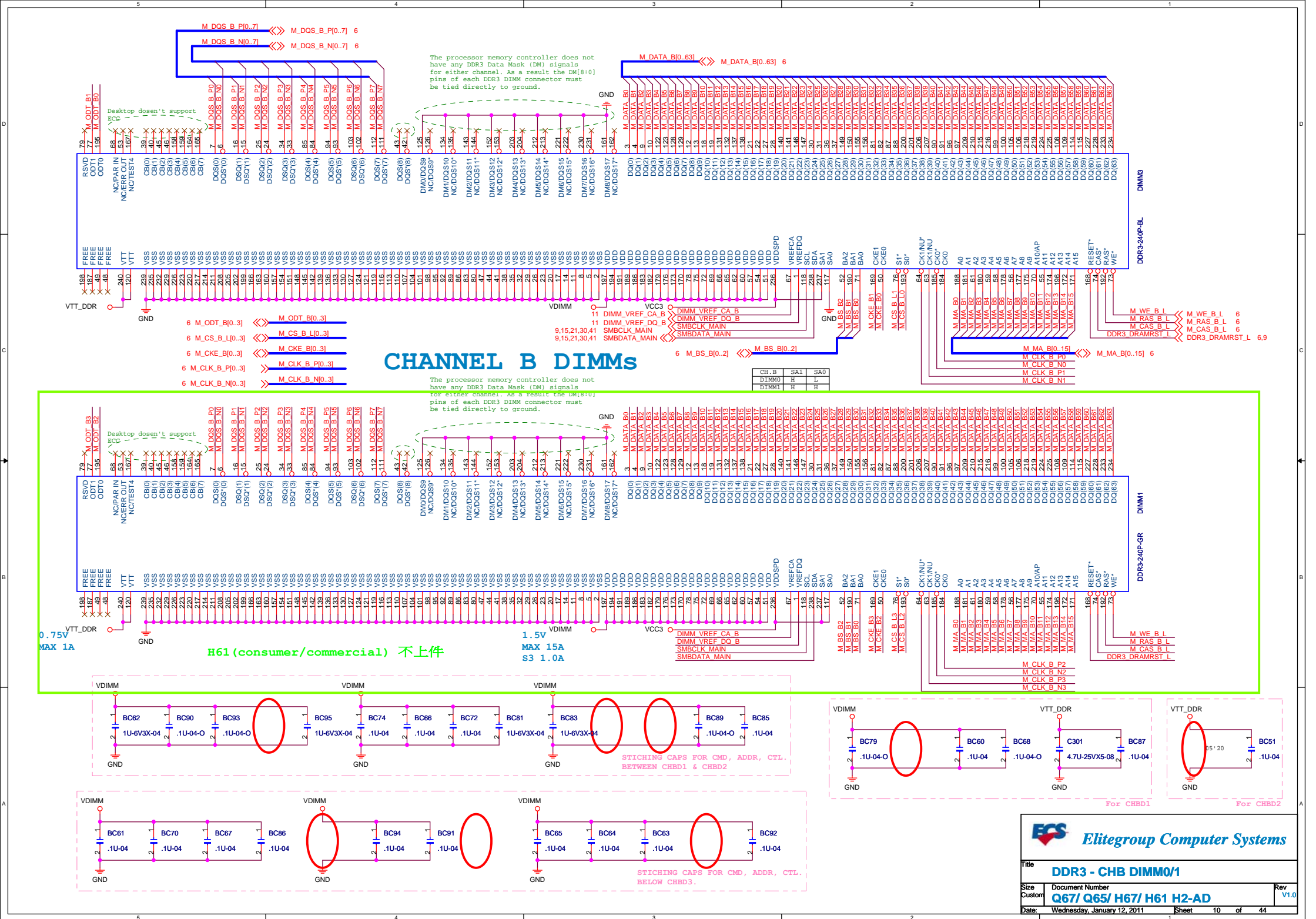
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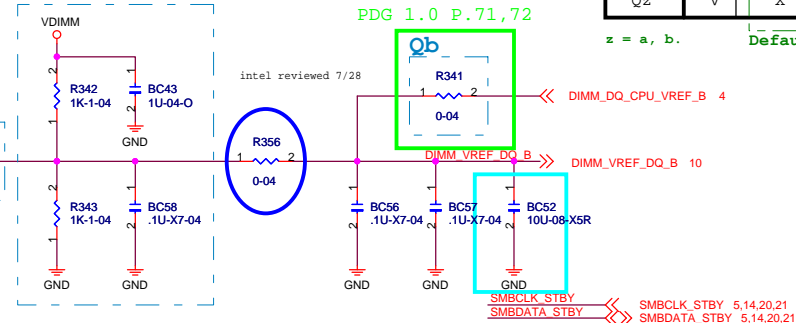
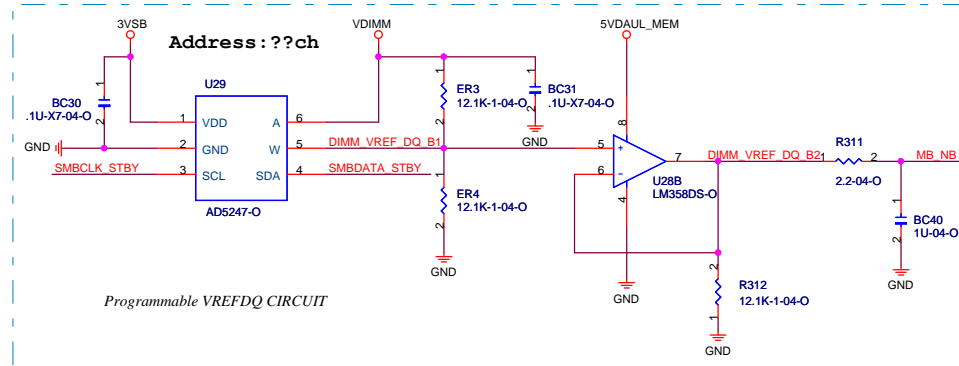
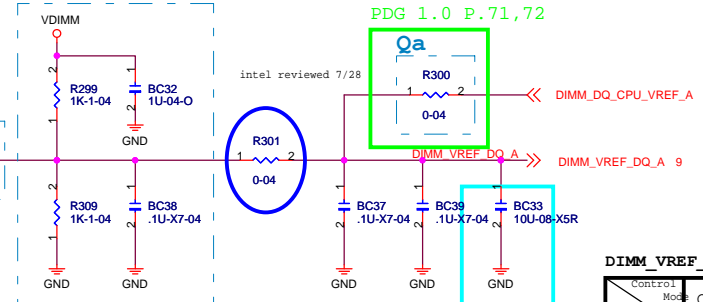
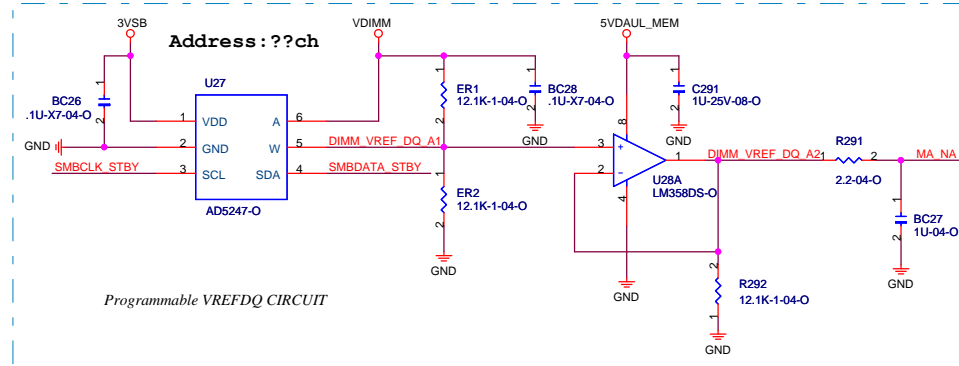
DDR_1
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Desktop doesn't support ECC



CPU1I				CPU1J			
BALLMAP_REV=1.4				BALLMAP_REV=1.4			
A17	VSS_001	VSS_091	AM27	AV11	VSS_181	VSS_271	G8
A23	VSS_002	VSS_092	AM3	AV14	VSS_182	VSS_272	H1
A26	VSS_003	VSS_093	AM30	AV17	VSS_183	VSS_273	H17
A29	VSS_004	VSS_094	AM36	AV3	VSS_184	VSS_274	H2
A35	VSS_005	VSS_095	AM37	AV35	VSS_185	VSS_275	H20
AA33	VSS_006	VSS_096	AM38	AV36	VSS_186	VSS_276	H23
AA34	VSS_007	VSS_097	AM39	AV6	VSS_187	VSS_277	H26
AA35	VSS_008	VSS_098	AM4	AW10	VSS_188	VSS_278	H29
AA36	VSS_009	VSS_099	AM40	AW11	VSS_189	VSS_279	H33
AA37	VSS_010	VSS_100	AM5	AW14	VSS_190	VSS_280	H35
AA38	VSS_011	VSS_101	AM10	AW16	VSS_191	VSS_281	H37
AB5	VSS_012	VSS_102	AN11	AW36	VSS_192	VSS_282	H39
AC1	VSS_013	VSS_103	AN17	AY11	VSS_193	VSS_283	H6
AC1	VSS_014	VSS_104	AN14	AY11	VSS_194	VSS_284	H5
AC6	VSS_015	VSS_105	AN19	AY14	VSS_195	VSS_285	H9
AD33	VSS_016	VSS_106	AN22	AY18	VSS_196	VSS_286	J11
AD36	VSS_017	VSS_107	AN24	AY35	VSS_197	VSS_287	J17
AD38	VSS_018	VSS_108	AN27	AY6	VSS_198	VSS_288	J20
AD39	VSS_019	VSS_109	AN30	AY8	VSS_199	VSS_289	J23
AD40	VSS_020	VSS_110	AN31	AY8	VSS_200	VSS_290	J26
AD5	VSS_021	VSS_111	AN32	B10	VSS_201	VSS_291	J29
AD8	VSS_022	VSS_112	AN33	B13	VSS_202	VSS_292	J32
AE3	VSS_023	VSS_113	AN34	B14	VSS_203	VSS_293	K1
AE33	VSS_024	VSS_114	AN35	B17	VSS_204	VSS_294	K12
AE36	VSS_025	VSS_115	AN36	B23	VSS_205	VSS_295	K13
AF1	VSS_026	VSS_116	AN5	B26	VSS_206	VSS_296	K14
AF34	VSS_027	VSS_117	AN6	B29	VSS_207	VSS_297	K17
AF36	VSS_028	VSS_118	AN8	B32	VSS_208	VSS_298	K2
AF37	VSS_029	VSS_119	AN9	B35	VSS_209	VSS_299	K20
AF40	VSS_030	VSS_120	AN7	B38	VSS_210	VSS_300	K23
AF5	VSS_031	VSS_121	AP1	B6	VSS_211	VSS_301	K26
AF6	VSS_032	VSS_122	AP11	C11	VSS_212	VSS_302	K29
AF7	VSS_033	VSS_123	AP14	C12	VSS_213	VSS_303	K33
AG36	VSS_034	VSS_124	AP17	C17	VSS_214	VSS_304	K35
AH2	VSS_035	VSS_125	AP22	C20	VSS_215	VSS_305	K37
AH3	VSS_036	VSS_126	AP25	C23	VSS_216	VSS_306	K39
AH33	VSS_037	VSS_127	AP27	C26	VSS_217	VSS_307	K5
AH36	VSS_038	VSS_128	AP30	C29	VSS_218	VSS_308	K6
AH37	VSS_039	VSS_129	AP36	C32	VSS_219	VSS_309	L10
AH38	VSS_040	VSS_130	AP37	C35	VSS_220	VSS_310	L17
AH40	VSS_041	VSS_131	AP4	C7	VSS_221	VSS_311	L20
AH5	VSS_042	VSS_132	AP40	C8	VSS_222	VSS_312	L23
AH8	VSS_043	VSS_133	AP5	D17	VSS_223	VSS_313	L26
AH12	VSS_044	VSS_134	AR11	D2	VSS_224	VSS_314	L29
AH15	VSS_045	VSS_135	AR14	D20	VSS_225	VSS_315	L8
AH18	VSS_046	VSS_136	AR17	D23	VSS_226	VSS_316	M17
AJ21	VSS_047	VSS_137	AR18	D26	VSS_227	VSS_317	M2
AJ25	VSS_048	VSS_138	AR19	D29	VSS_228	VSS_318	M20
AJ25	VSS_049	VSS_139	AR27	D32	VSS_229	VSS_319	M23
AJ27	VSS_050	VSS_140	AR30	D37	VSS_230	VSS_320	M26
AJ36	VSS_051	VSS_141	AR36	D38	VSS_231	VSS_321	M29
AJ5	VSS_052	VSS_142	AT1	D4	VSS_232	VSS_322	M33
AK1	VSS_053	VSS_143	AT5	D5	VSS_233	VSS_323	M35
AK10	VSS_054	VSS_144	AT10	D9	VSS_234	VSS_324	M37
AK13	VSS_055	VSS_145	AT12	E11	VSS_235	VSS_325	M39
AK14	VSS_056	VSS_146	AT13	E12	VSS_236	VSS_326	M5
AK16	VSS_057	VSS_147	AT15	E17	VSS_237	VSS_327	M6
AK22	VSS_058	VSS_148	AT16	E20	VSS_238	VSS_328	M9
AK28	VSS_059	VSS_149	AT17	E23	VSS_239	VSS_329	N8
AK31	VSS_060	VSS_150	AT2	E26	VSS_240	VSS_330	P1
AK32	VSS_061	VSS_151	AT25	E29	VSS_241	VSS_331	P2
AK33	VSS_062	VSS_152	AT28	E32	VSS_242	VSS_332	P36
AK34	VSS_063	VSS_153	AT29	E36	VSS_243	VSS_333	P38
AK35	VSS_064	VSS_154	AT32	F7	VSS_244	VSS_334	P40
AK36	VSS_065	VSS_155	AT3	E8	VSS_245	VSS_335	P5
AK37	VSS_066	VSS_156	AT30	F1	VSS_246	VSS_336	P6
AK4	VSS_067	VSS_157	AT31	F10	VSS_247	VSS_337	P33
AK40	VSS_068	VSS_158	AT32	F13	VSS_248	VSS_338	R35
AK5	VSS_069	VSS_159	AT33	F14	VSS_249	VSS_339	R37
AK6	VSS_070	VSS_160	AT34	F17	VSS_250	VSS_340	R39
AK7	VSS_071	VSS_161	AT35	F2	VSS_251	VSS_341	R8
AK8	VSS_072	VSS_162	AT36	F20	VSS_252	VSS_342	T1
AK9	VSS_073	VSS_163	AT37	F23	VSS_253	VSS_343	T5
AL11	VSS_074	VSS_164	AT38	F26	VSS_254	VSS_344	T6
AL14	VSS_075	VSS_165	AT39	F29	VSS_255	VSS_345	U8
AL17	VSS_076	VSS_166	AT4	F35	VSS_256	VSS_346	U1
AL19	VSS_077	VSS_167	AT40	F37	VSS_257	VSS_347	V1
AL24	VSS_078	VSS_168	AT5	F39	VSS_258	VSS_348	V2
AL27	VSS_079	VSS_169	AT6	F5	VSS_259	VSS_349	V33
AL30	VSS_080	VSS_170	AT7	F6	VSS_260	VSS_350	V35
AL36	VSS_081	VSS_171	AT8	F9	VSS_261	VSS_351	V36
AL5	VSS_082	VSS_172	AT9	G11	VSS_262	VSS_352	V37
AM1	VSS_083	VSS_173	AT10	G12	VSS_263	VSS_353	V38
AM11	VSS_084	VSS_174	AT15	G17	VSS_264	VSS_354	V39
AM14	VSS_085	VSS_175	AT26	G20	VSS_265	VSS_355	V40
AM2	VSS_086	VSS_176	AT34	G23	VSS_266	VSS_356	V5
AM2	VSS_087	VSS_177	AT3	G26	VSS_267	VSS_357	W6
AM21	VSS_088	VSS_178	AT6	G29	VSS_268	VSS_358	Y5
AM23	VSS_089	VSS_179	AT8	G34	VSS_269	VSS_359	Y8
AM25	VSS_090	VSS_180	AV10	G7	VSS_270	VSS_360	
A4	VSS_NCTF_01			AY37	VSS_NCTF_03		
AV39	VSS_NCTF_02	9 OF 10		B3	VSS_NCTF_04	10 OF 10	
GND				GND			
SKT_H2_CRB				SKT_H2_CRB			
GND				GND			

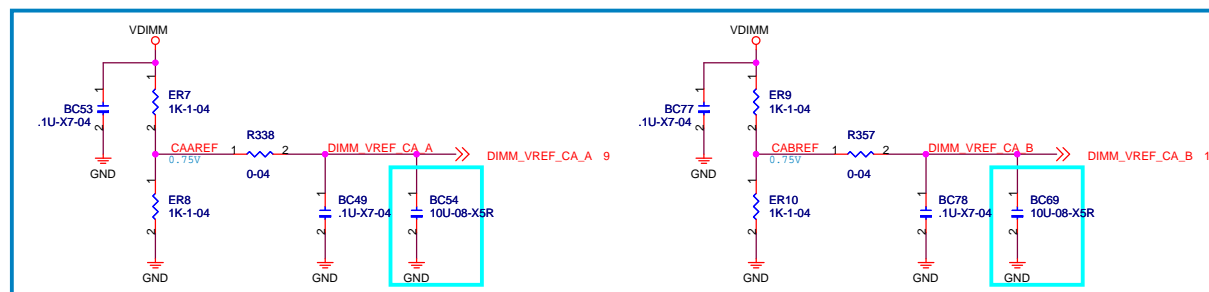




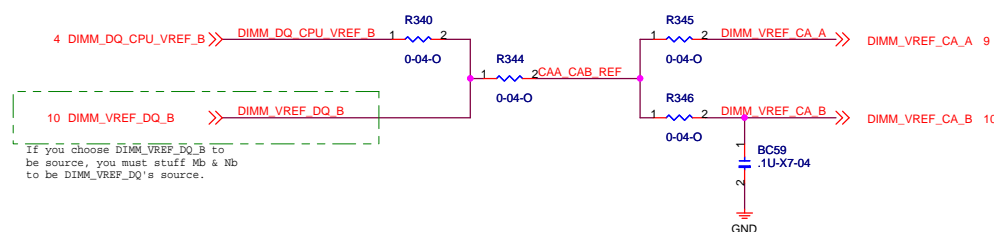
Control Mode Part	CPU	Divider	PCH + Controller
Mz	X	X	V
Nz	X	X	V
Pz	X	V	X
Qz	V	X	X

```
z = a, b.      | _ _ _ |
                | Default
```

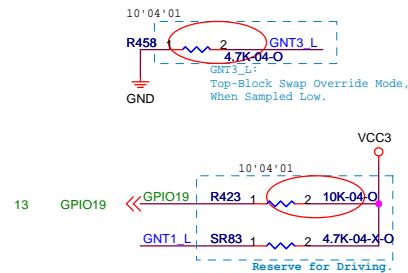
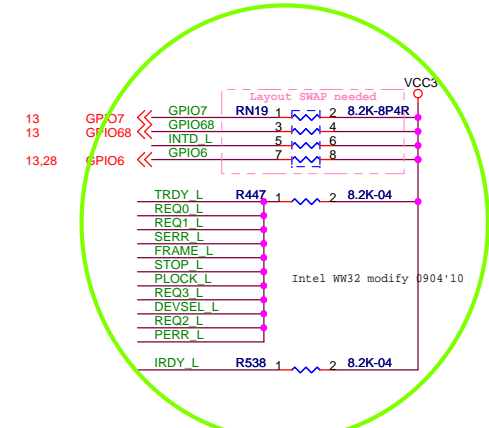
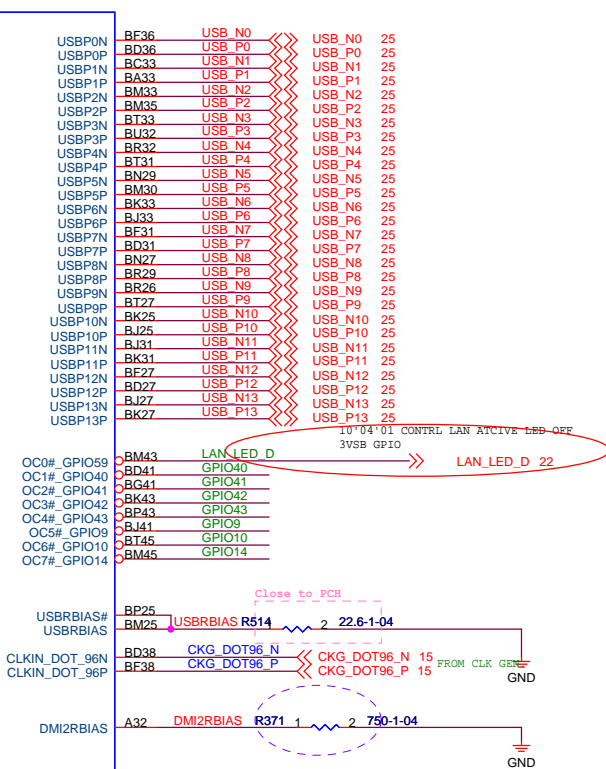
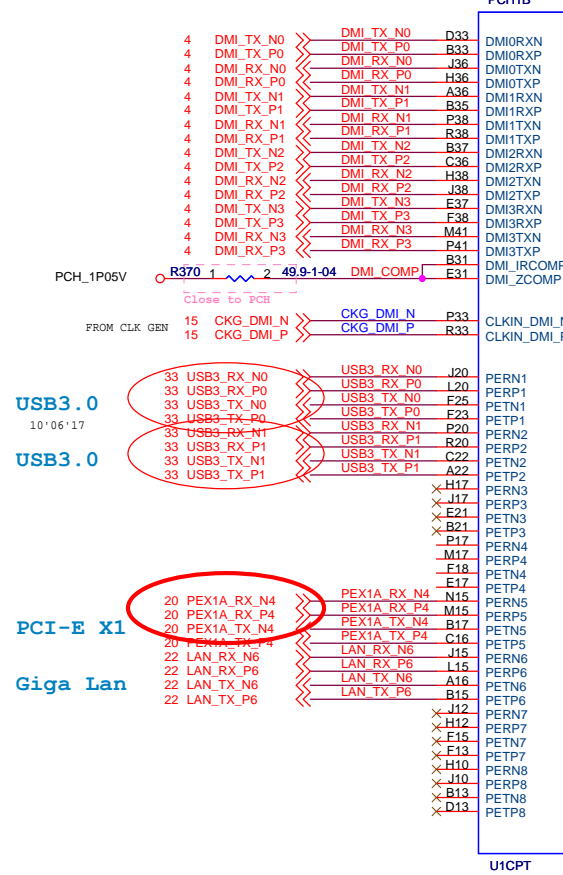
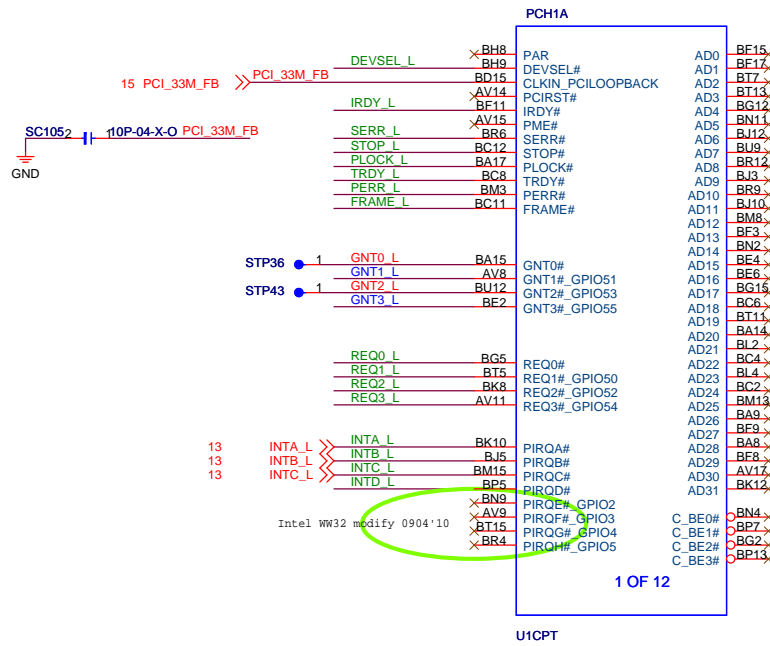
DIMM VREF DQ Control Circuit



DIMM VREF CA Circuit



If you choose DIMM_VREF_DQ_B to be source, you must stuff Mb & Nb to be DIMM VREF DQ's source.

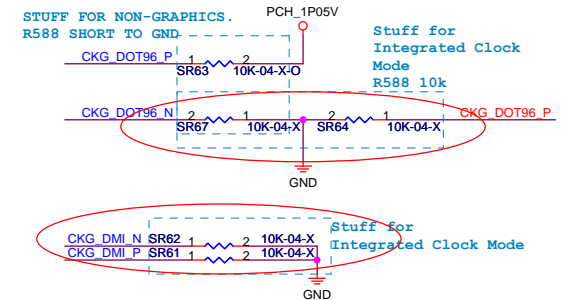
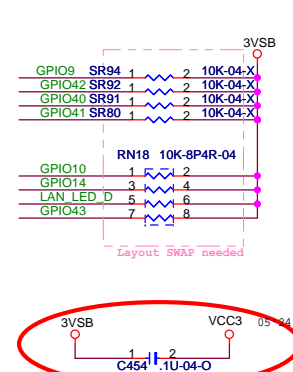


Boot Device Select:

BOOT DEVICE	GNT1_L	GPIO19
LPC	0	0
PCI	1	0
SPI	1	1

* GNT[0..3]#
GPIO19
have been internal pull high to +VCC3

GNT1#, GPIO19 Follow CPT EDS V0.7,
CRB V0.7, PDG V0.8

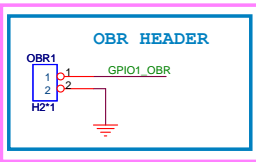


Eli Computer Systems

Title	PCH - DMI/PCI/PE/USB		
Size	Document Number	Q67/ Q65/ H67/ H61 H2-AD	
Custom			Rev V1.0
Date:	Wednesday, January 12, 2011	Sheet 12 of 44	

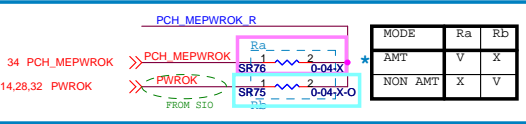
Q67/Q65/H61 (commercial) 上件

H67/H61 (consumer) 上件

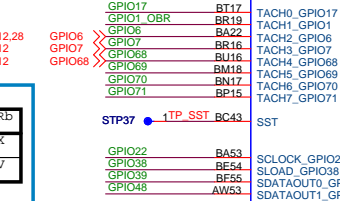
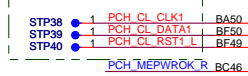


Q67/Q65上件

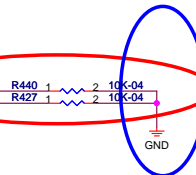
H67/H61 (consumer/commercial) 上件



MOBILE ONLY, NOT FOR DESKTOP.
CRB CONNECT TO MINI PCIe.



FAN FUNCTION JUST FOR MOBILE



Intel received and modify again
07'29'10

INIT3_3V_L R485 1 2 1K-04-O

Stuff for
Integrated Clock Mode

05'09'10

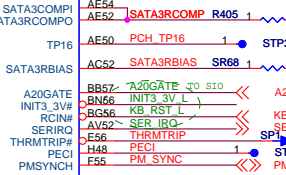
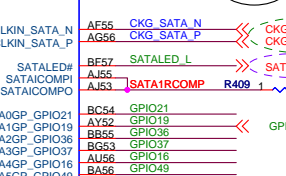
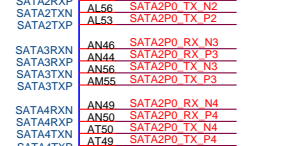
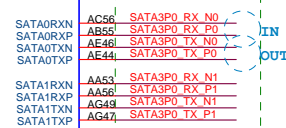
CKG_SATA_N SR66 1 2 10K-04-X

CKG_SATA_P SR65 1 2 10K-04-X

3 OF 12

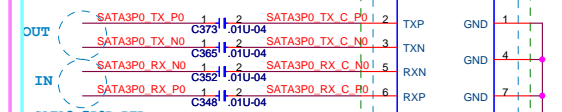
U1CPT

ONLY SATA PORT0 & PORT1 SUPPORT SATA3.0,
ALSO SUPPORT SATA2.0, SATA1.0.



PECI SIGNAL, CRB RESERVE CONNECT FROM CPU

ONLY SATA PORT0 & PORT1 SUPPORT SATA3.0,
ALSO SUPPORT SATA2.0, SATA1.0.

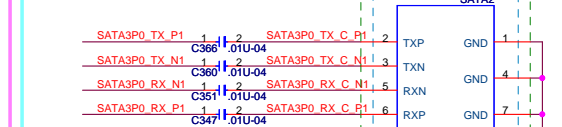


SATA3-7P2R-RED

XX-XXX-XXXXXX

Footprint: SATA3_7P-LOTES

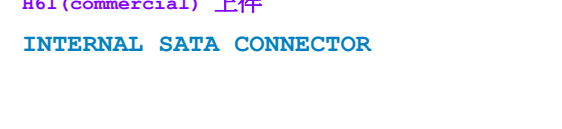
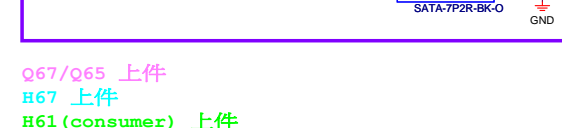
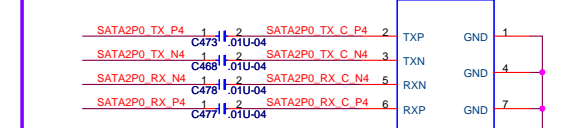
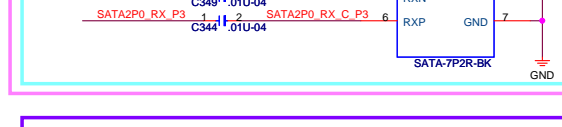
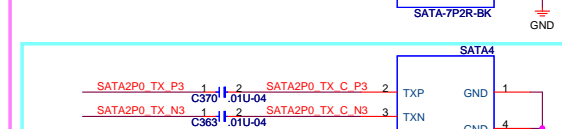
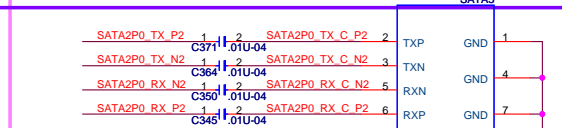
Sample Request!



Layout Note:

SATA3.0 4.5/7.5/20 in 90 Q ±17.5%

SATA2.0 4.5/7.5/15 in 90 Q ±17.5%



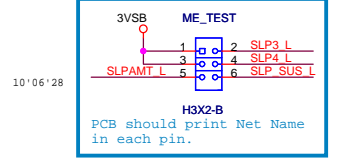
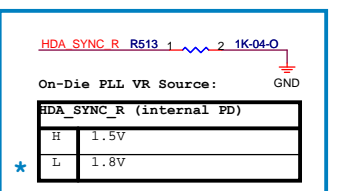
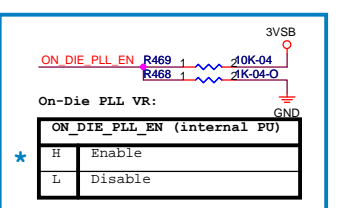
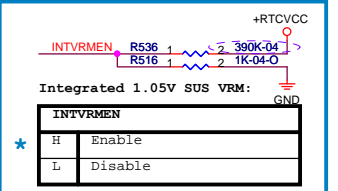
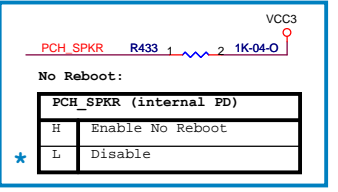
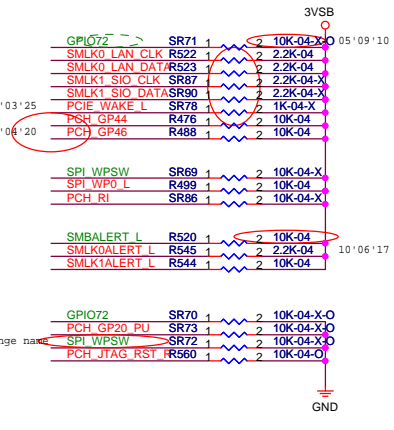
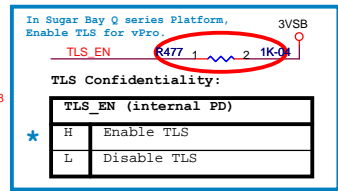
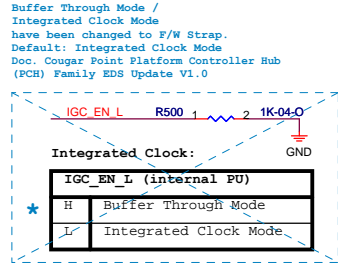
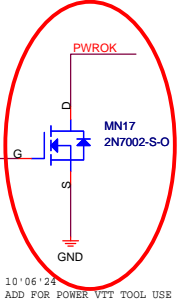
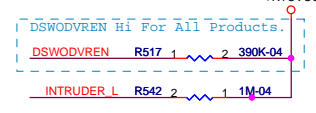
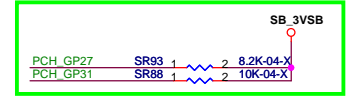
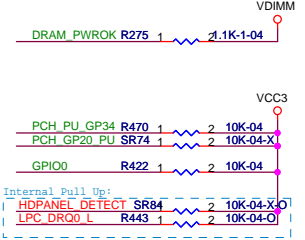
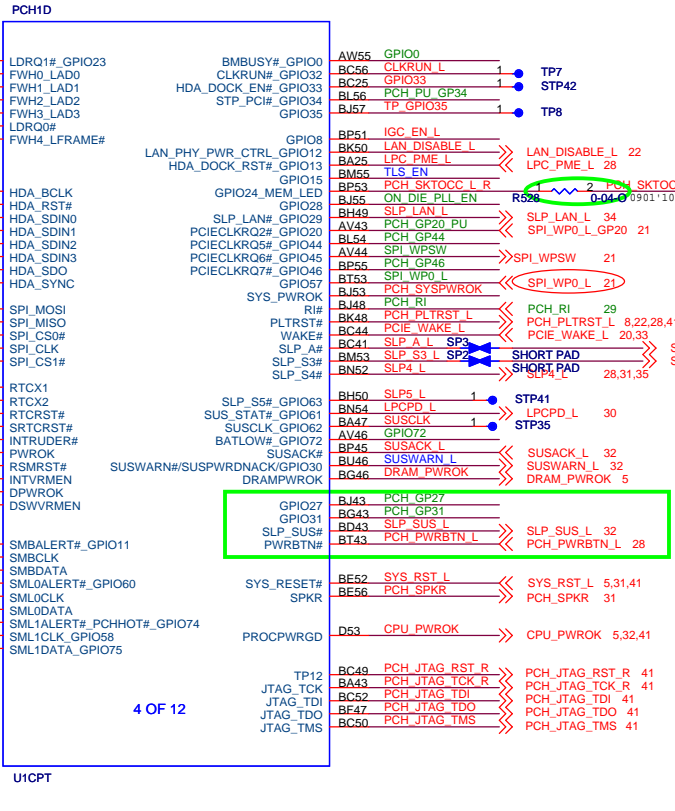
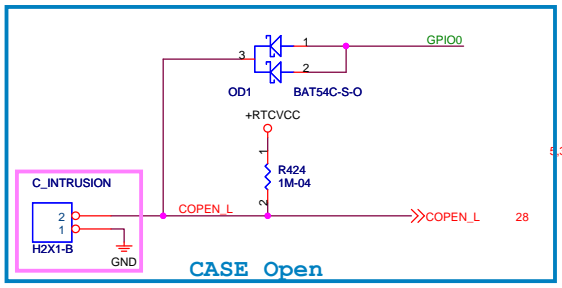
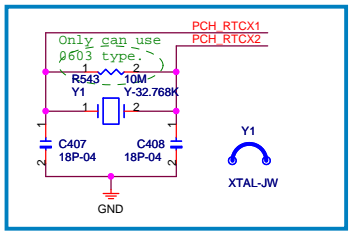
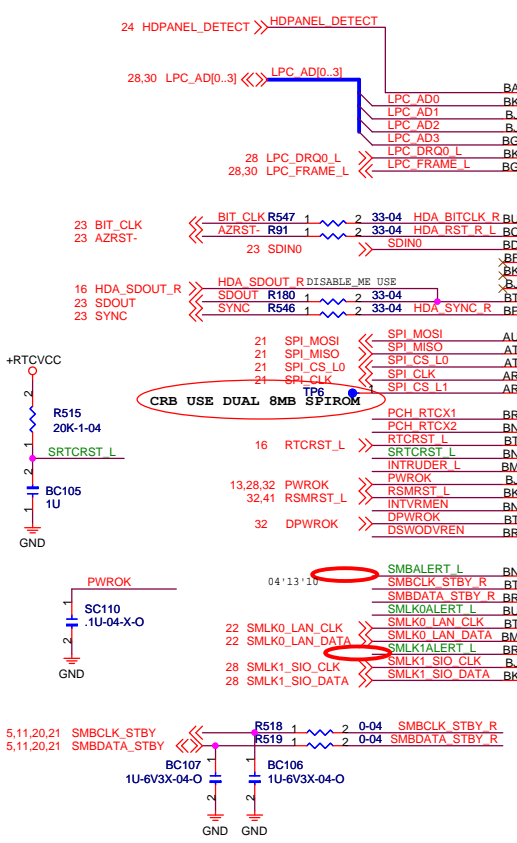
Q67/Q65 上件

H67 上件

H61 (consumer) 上件

H61 (commercial) 上件

INTERNAL SATA CONNECTOR



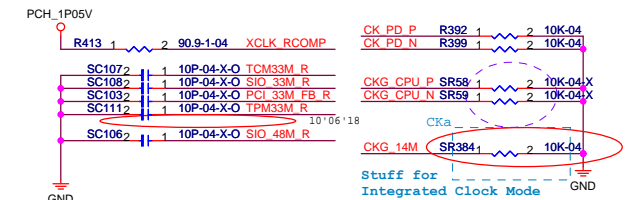
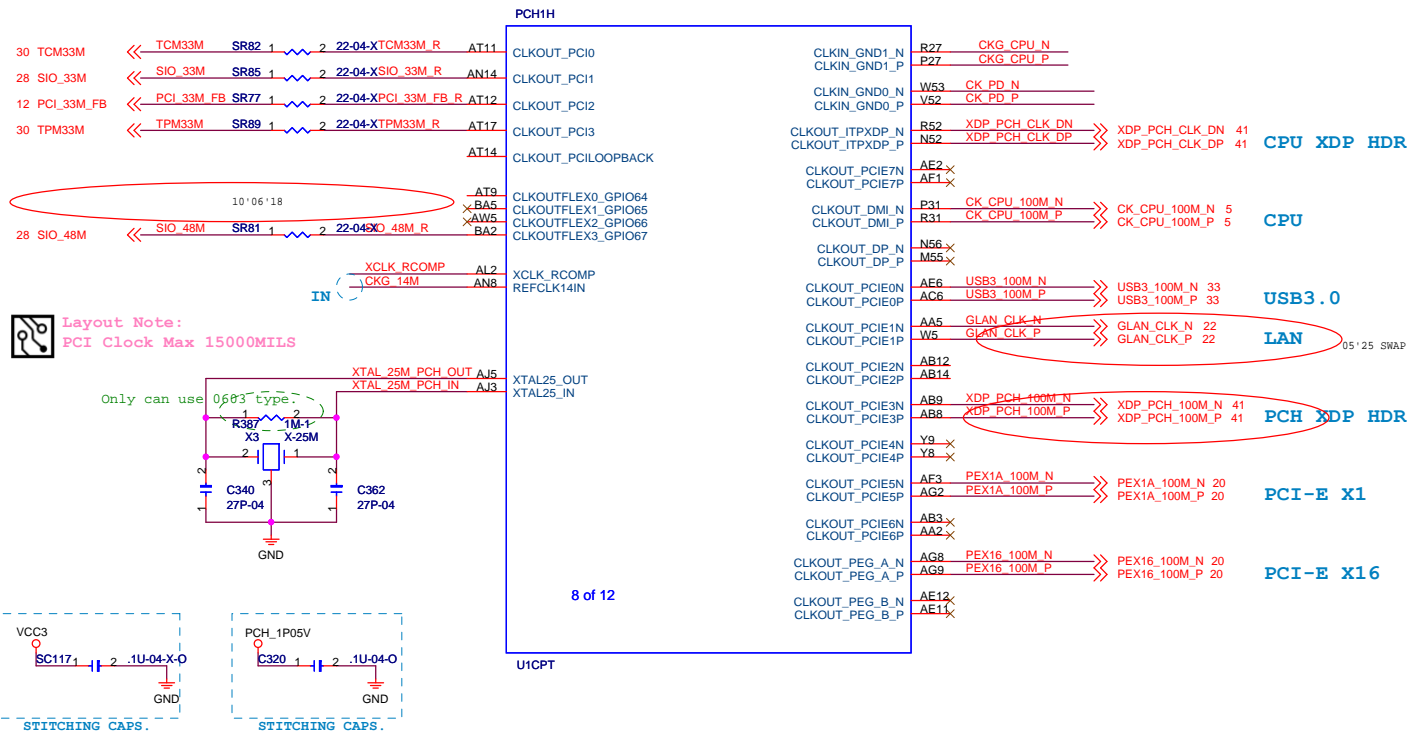
ME Test Header

VCC3	S3_L
S5_L	S4_L
SA_L	GND

Layout Note:
Print this table
near ME_TEST

0908'10 TAKE OFF CLK GEN

CLK GEN.Seligo SLG421 Circuit.



05'25 SWAP

05'25 SWAP

10'03'24

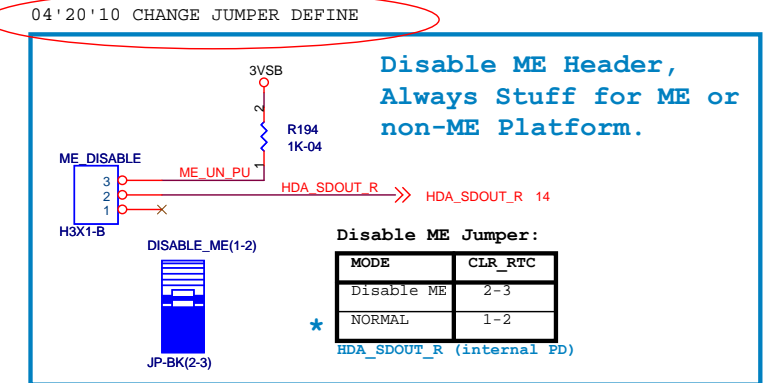
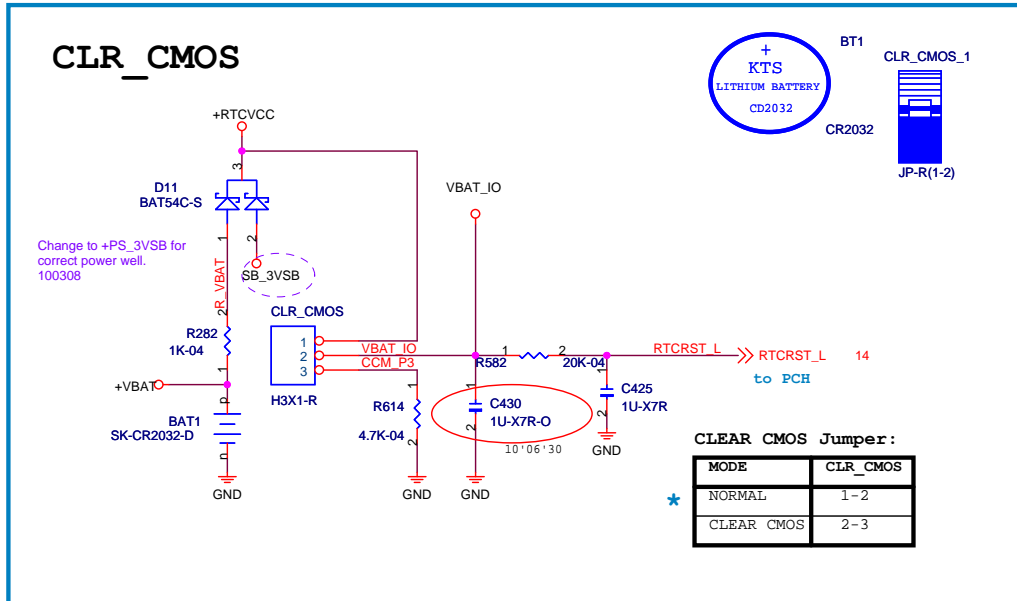
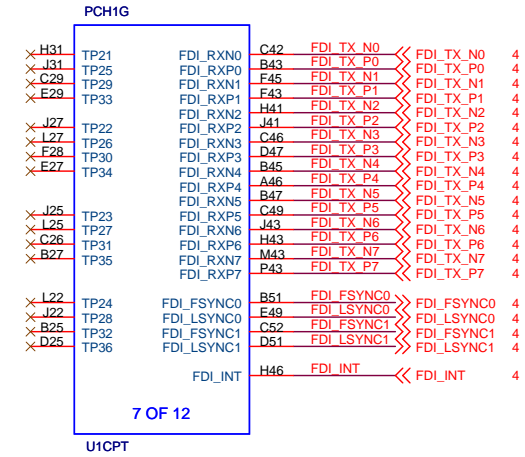
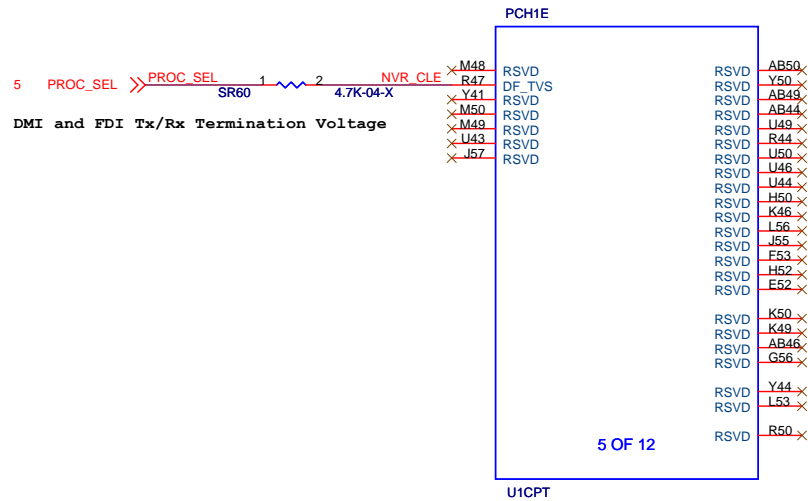
★

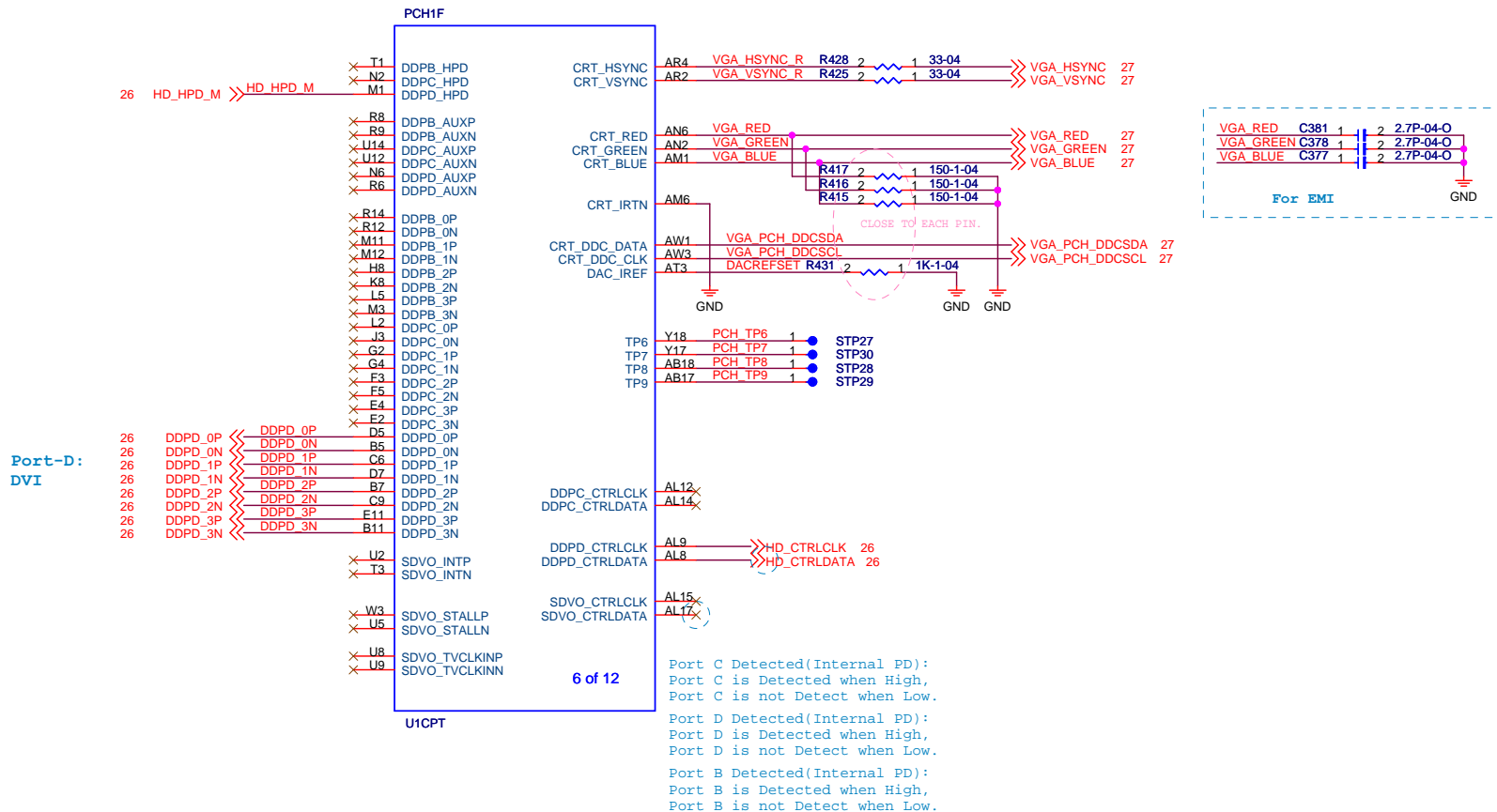
Clock Mode	CLK GEN. Seligo SLG421 Circuit..	CKa
Integrated Clock Mode	x	v
Buffer Through Mode	y	x

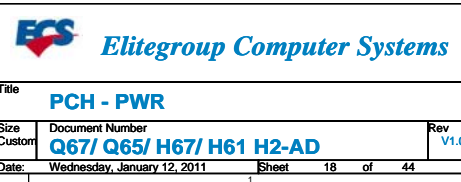


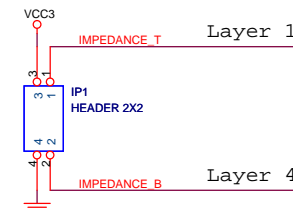
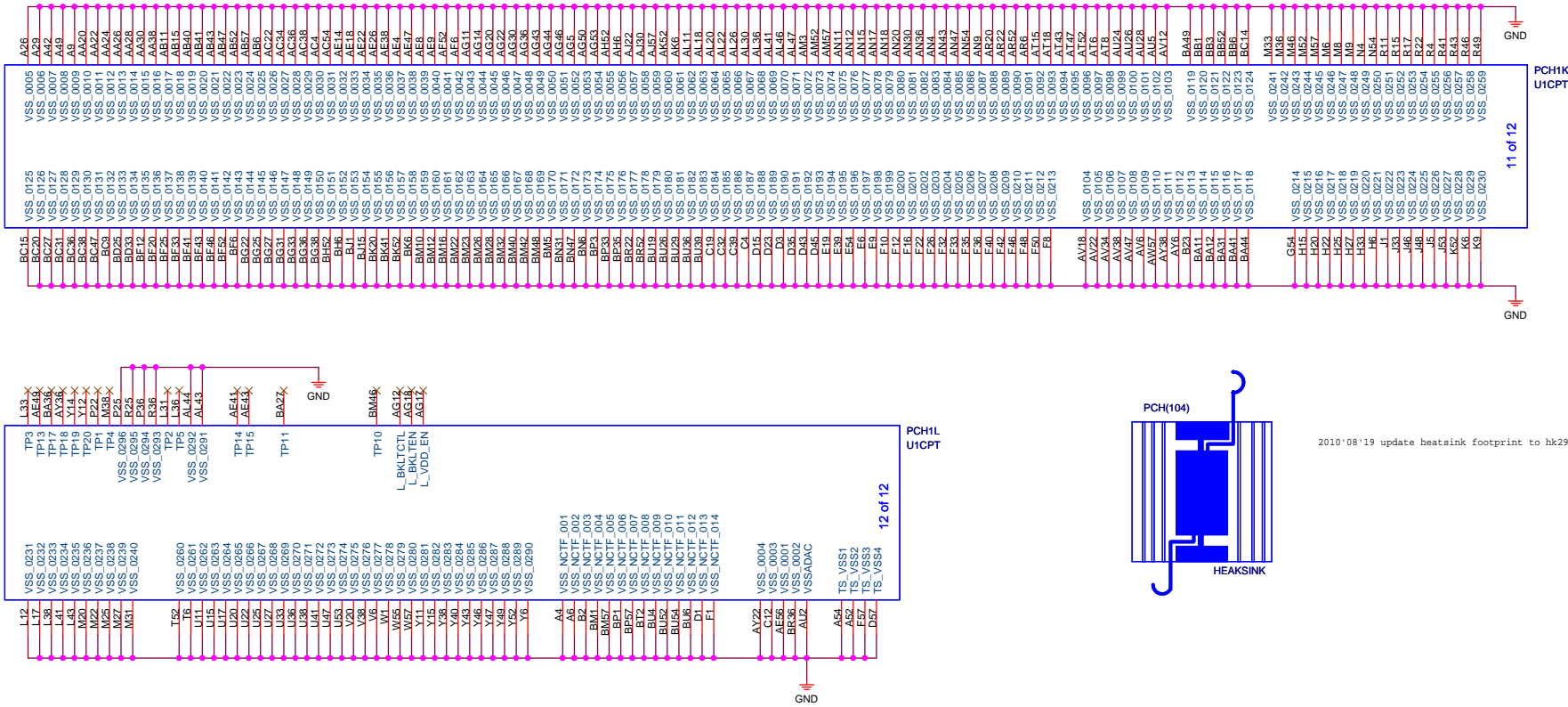
Elitegroup Computer Systems

Title			PCH - CLK IO, CKG - SLG421
Size	Document Number	Rev	
Custom	Q67/ Q65/ H67/ H61 H2-AD	V1.0	
Date:	Wednesday, January 12, 2011	Sheet	15 of 44



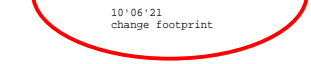




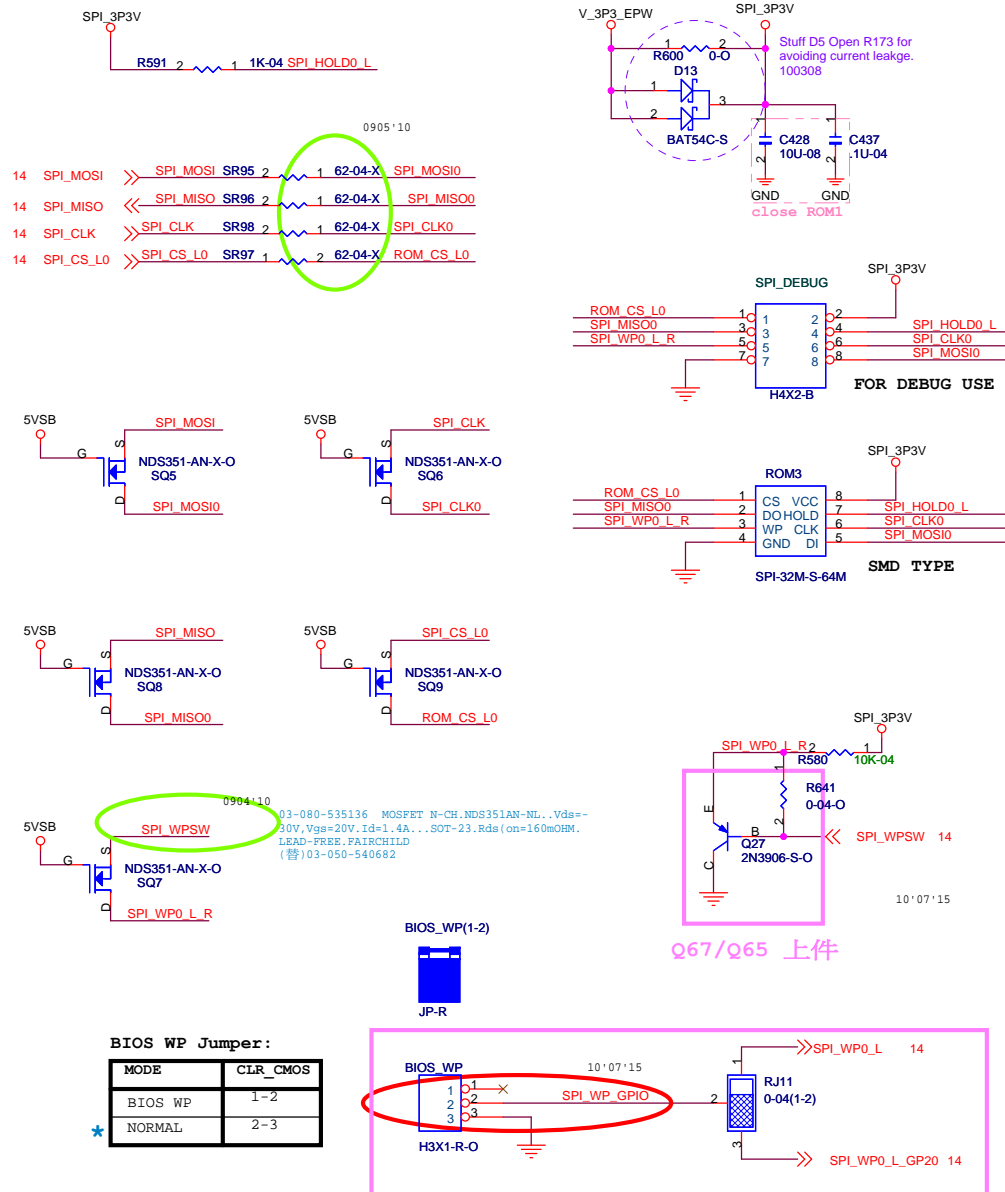


10'06'18 FOR Level Shift

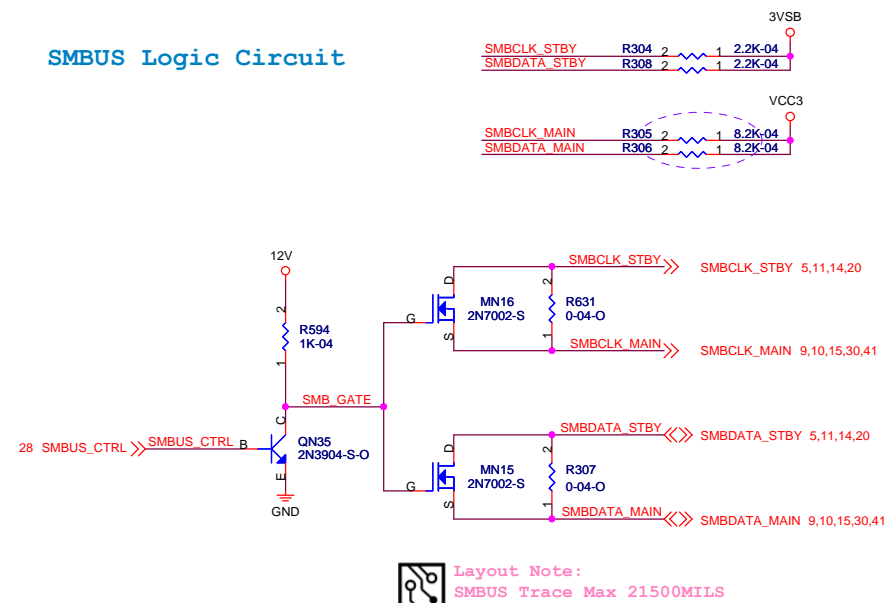
26 PEG_PINB4 <<< PEG
5,11,14,21 SMBCLK_STBY <<< SM
5,11,14,21 SMBDATA_STBY <<< SM



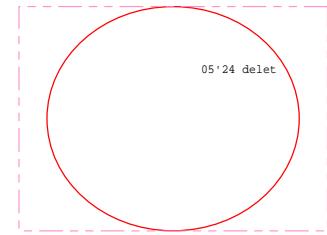
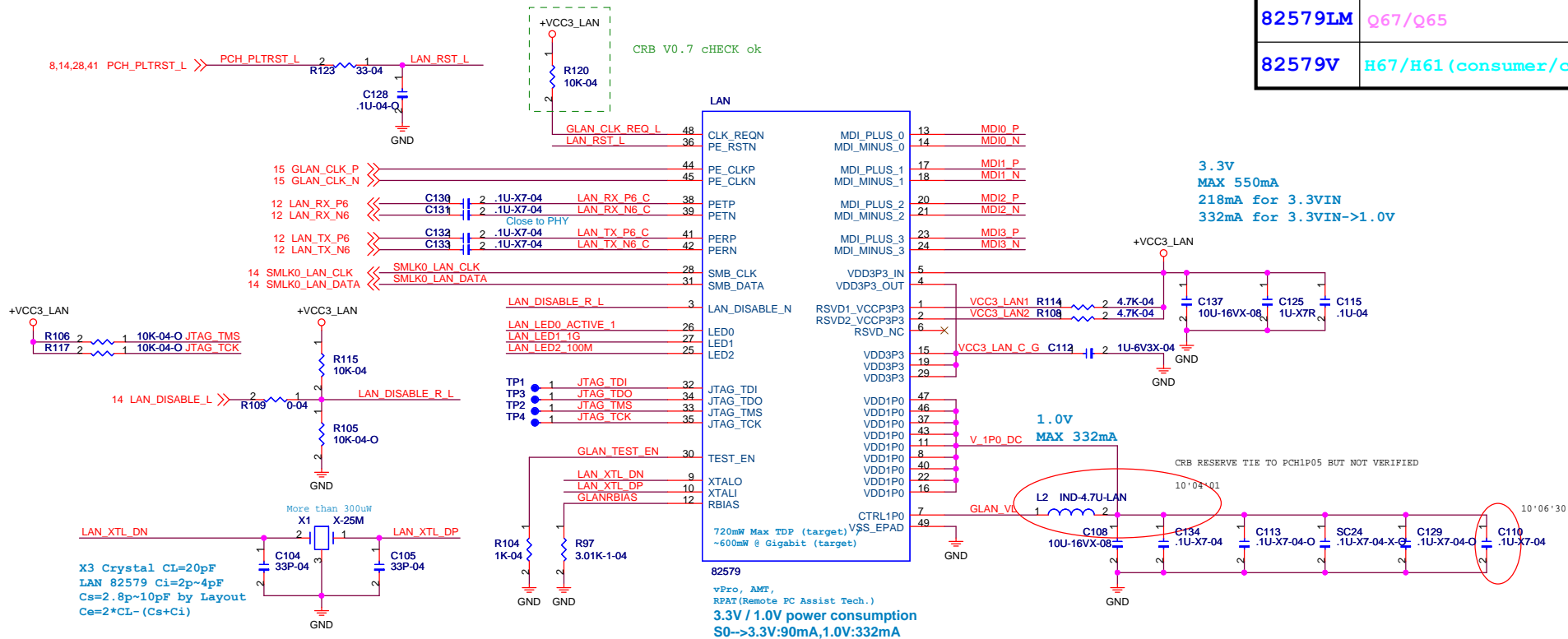
SPI ROM Circuit



SMBUS Logic Circuit




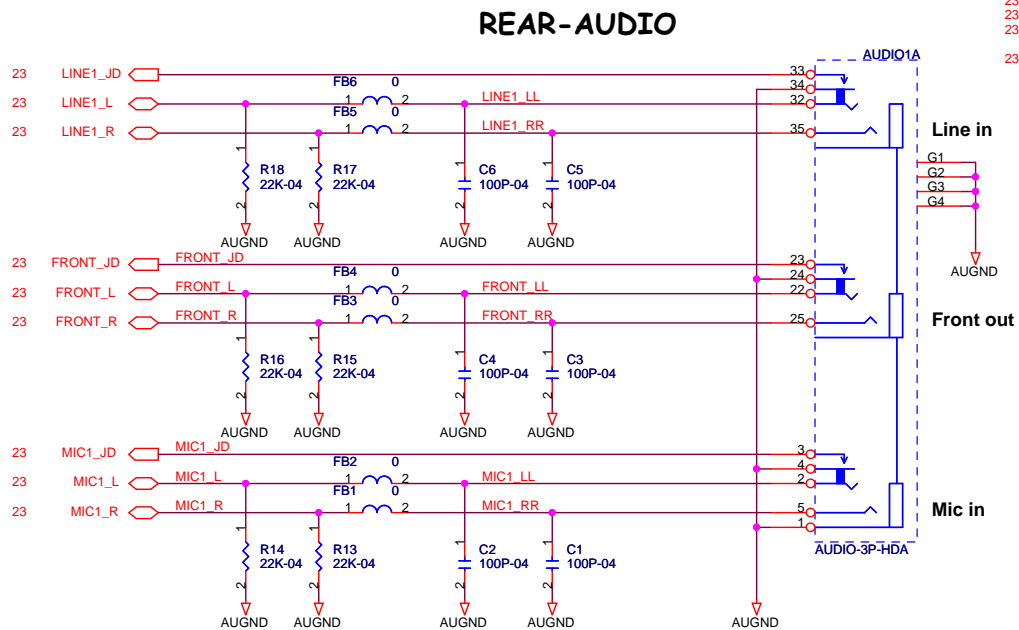
82579LM	Q67/Q65
82579V	H67/H61 (consumer/commercial) 上件



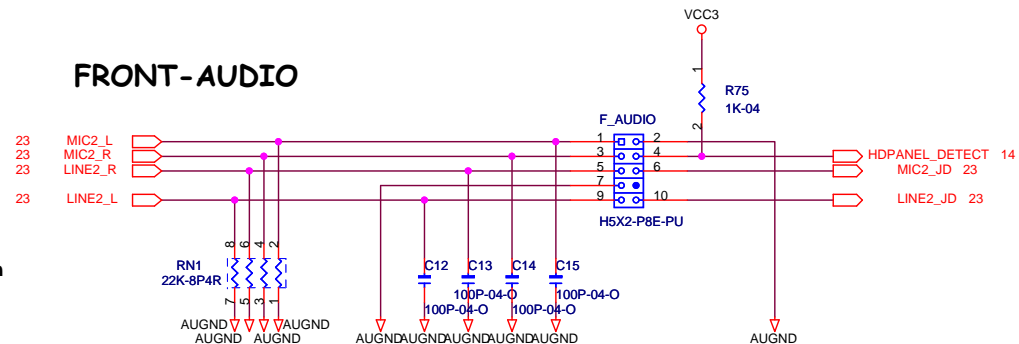
Place Caps between chipset and Lan connector in Bottom Side.

Title LAN PHY - 82579, USBLAN		
Size Custom	Document Number Q67/ Q65/ H67/ H61 H2-AD	Rev V1.0
Date: Wednesday, January 12, 2011	Sheet 22	of 44

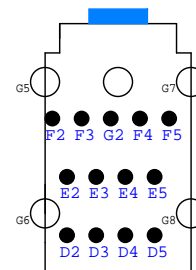
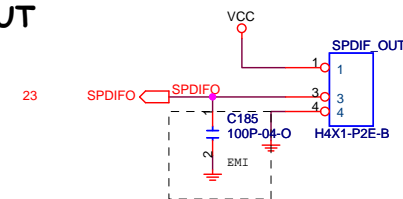
 Elitegroup Computer Systems			
Title			
AUDIO ALC662 (CHIP)			
Size	Document Number		Rev
Custom	Q67/ Q65/ H67/ H61 H2-AD		V1.0
Date:	Wednesday, January 12, 2011	Sheet	23 of 44



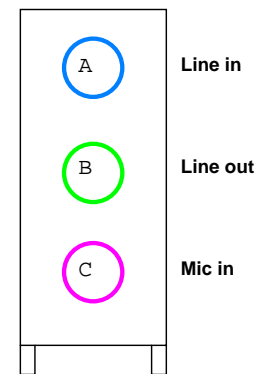
FRONT-AUDIO



SPDIF-OUT



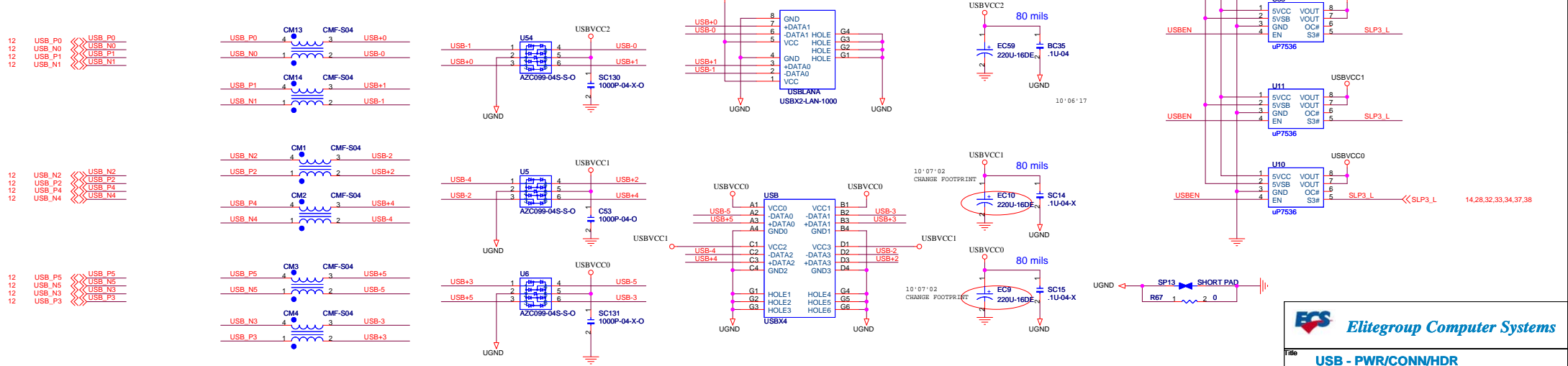
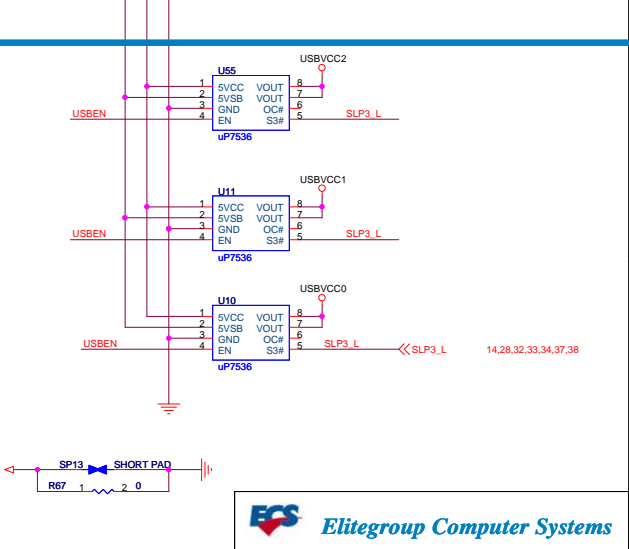
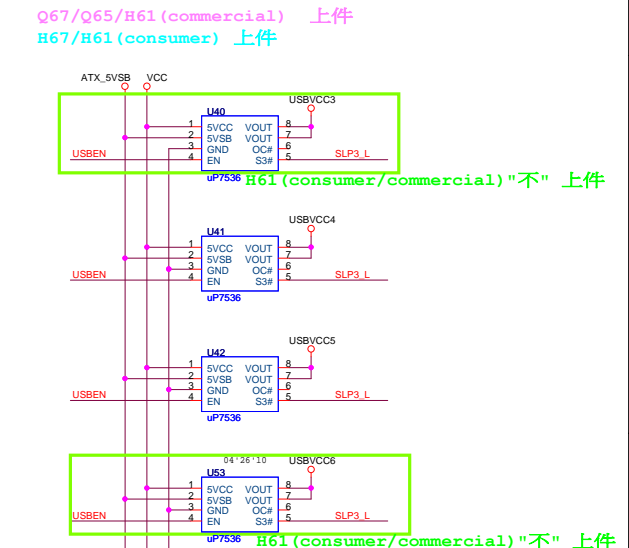
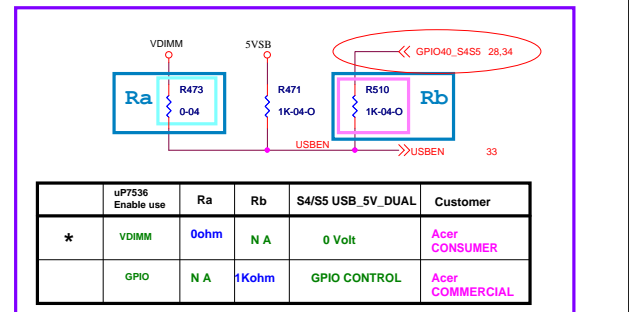
TOP VIEW



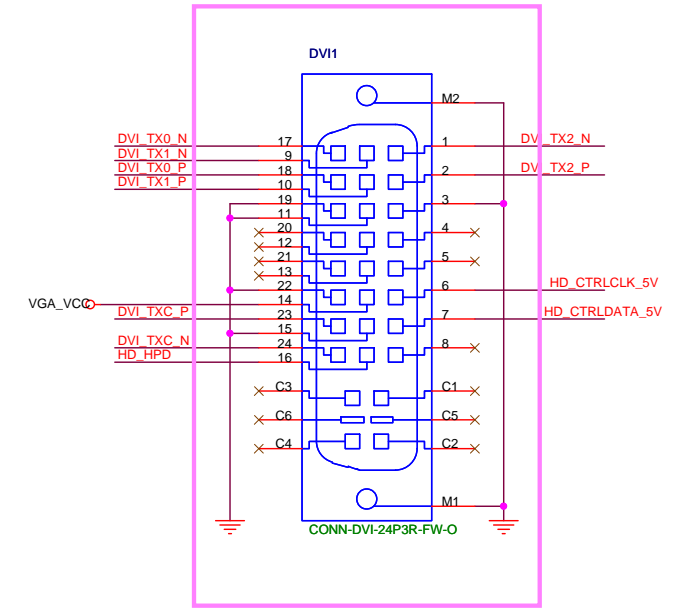
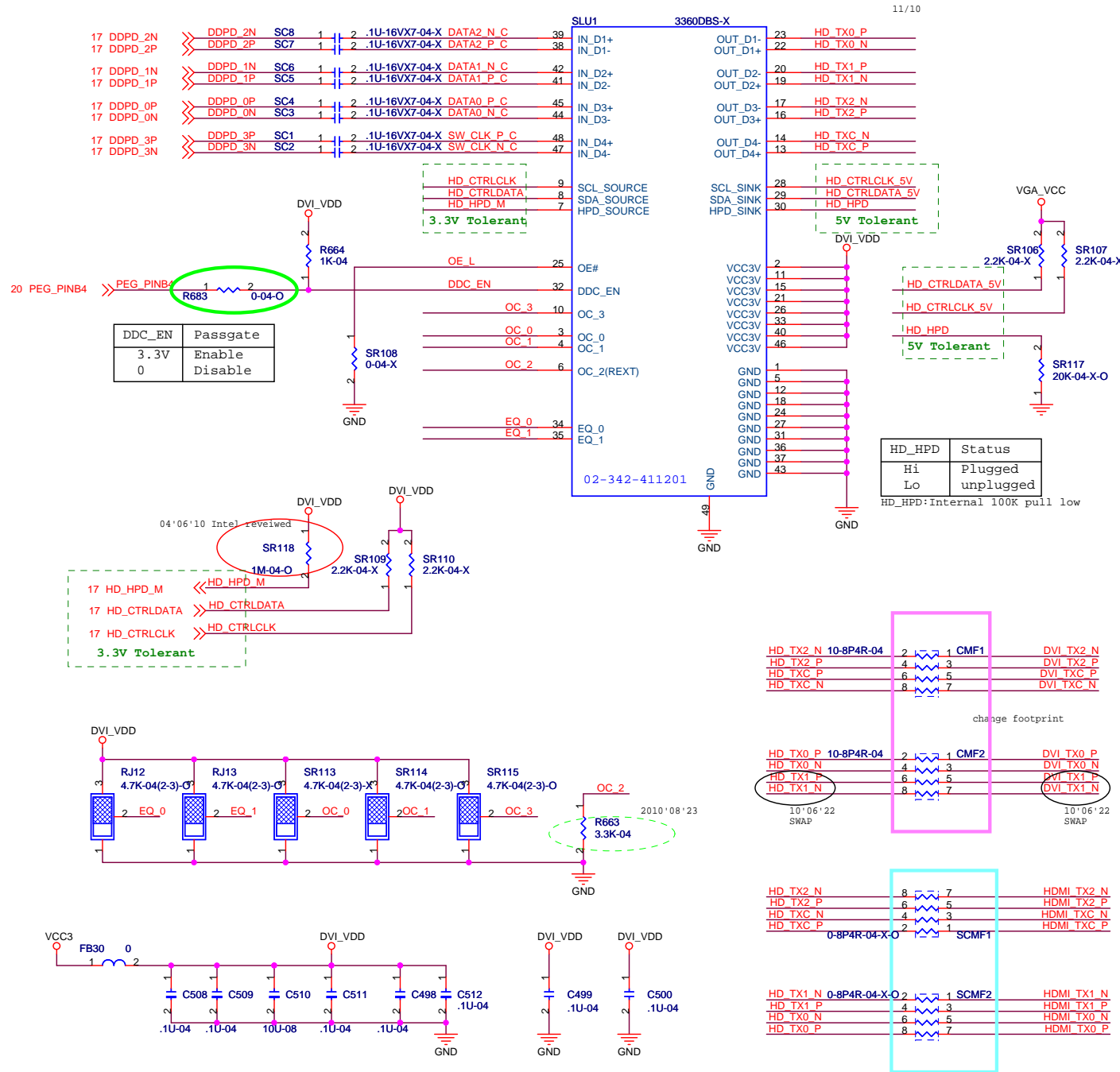
FRONT VIEW

Elitegroup Computer Systems

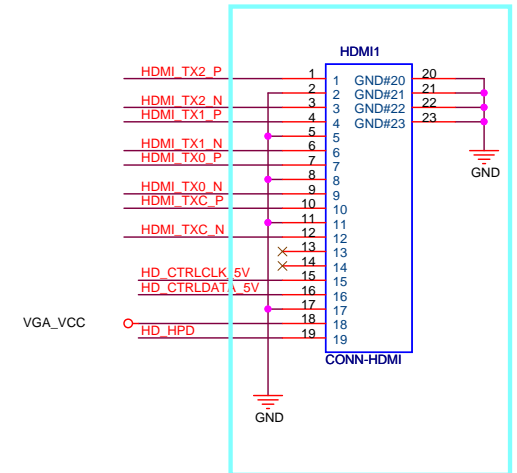
Title		
AUDIO ALC662 (PANEL)		
Size	Document Number	Rev
B	Q67/ Q65/ H67/ H61 H2-AD	V1.0
Date:	Wednesday, January 12, 2011	Sheet 24 of 44

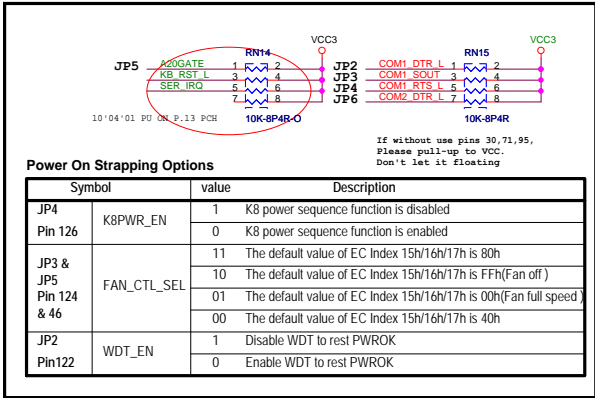


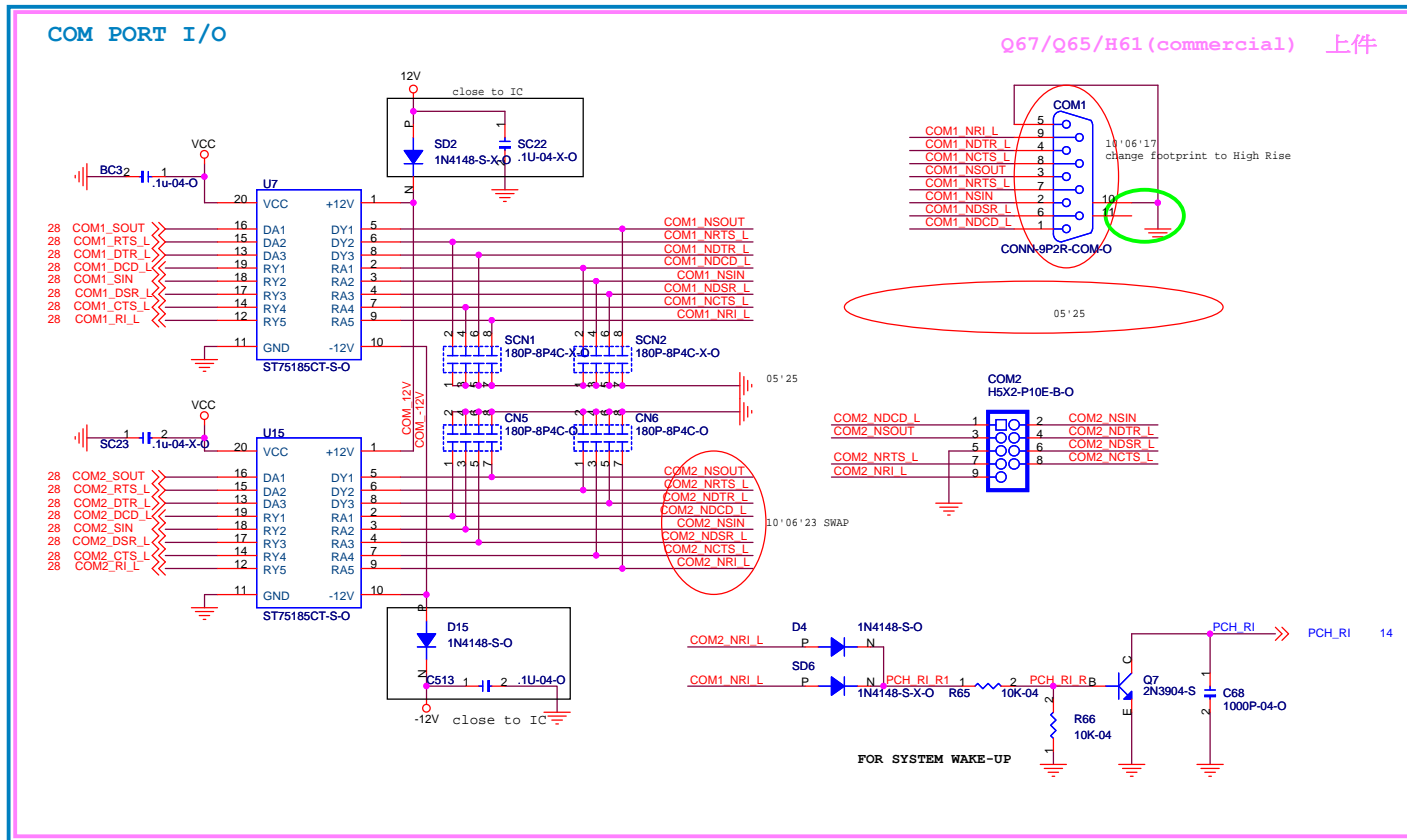
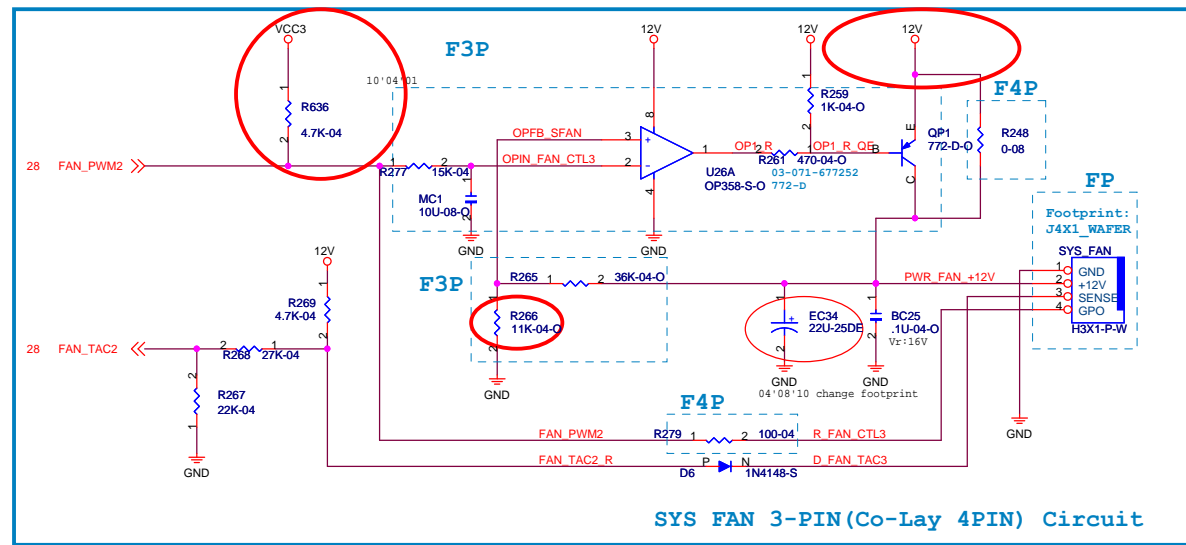
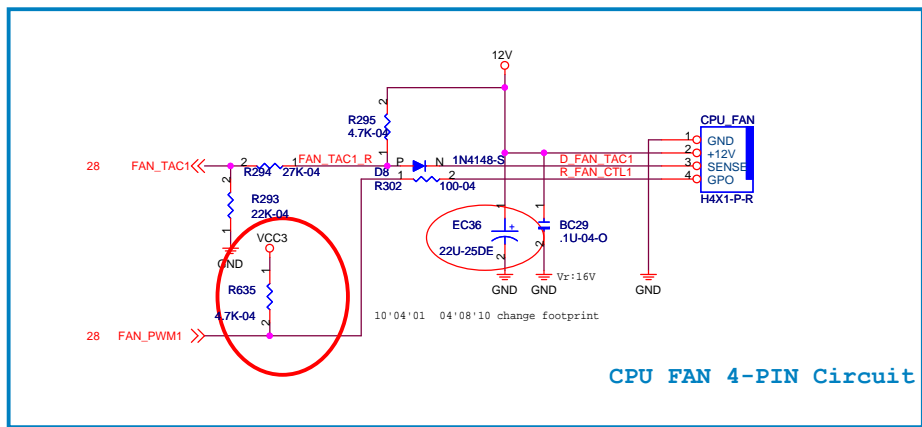
Level Shifter



Q67/Q65/H61 (commercial) 上件
H67/H61 (consumer) 上件

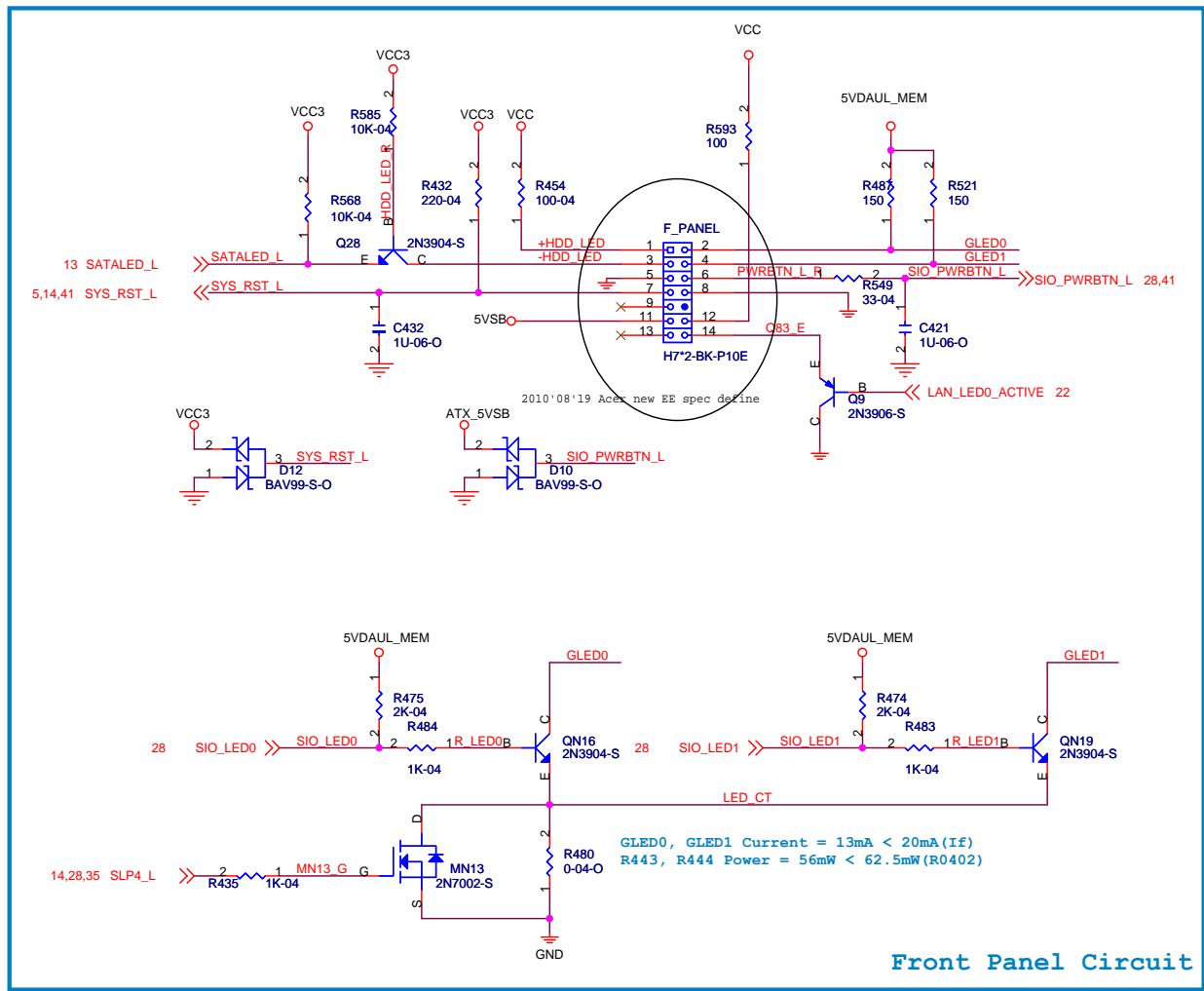






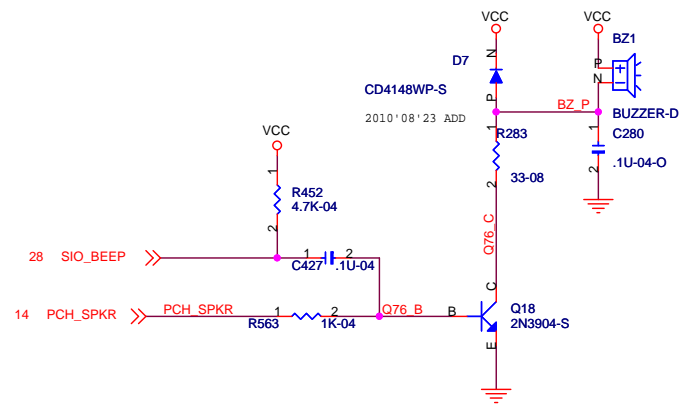
PWR FAN:

MODE	F3P	F4P	FP Value
3PIN	V	X	H3X1-P-W
4PIN	X	V	H4X1-P-W



Front Panel Circuit

Buzzer Circuit



Elitegroup Computer Systems

Title

F_PANEL, BUZ

Size

Document Number

Q67/ Q65/ H67/ H61 H2-AD

Rev

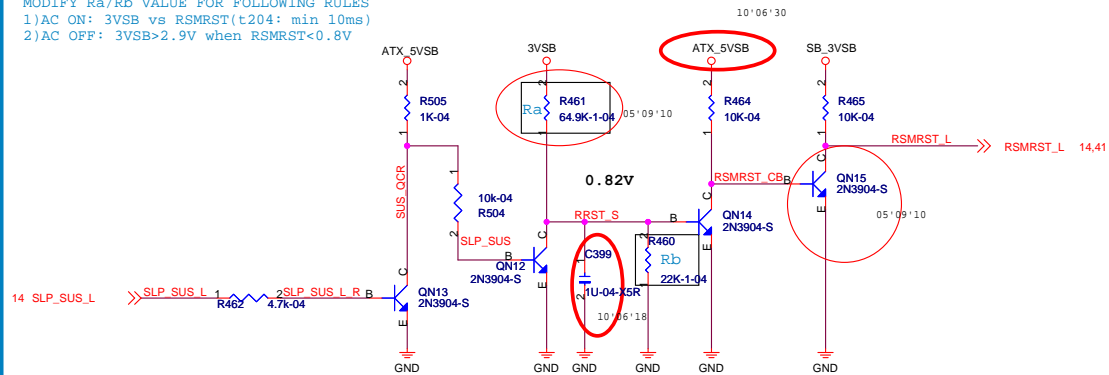
V1.0

Date: Wednesday, January 12, 2011

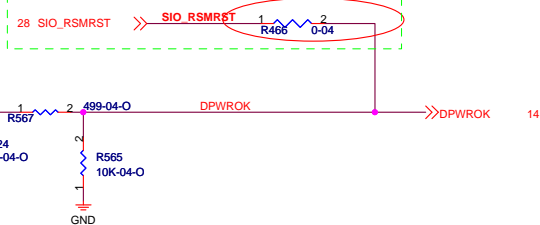
Sheet 31 of 44

MODIFY Ra/Rb VALUE FOR FOLLOWING RULES

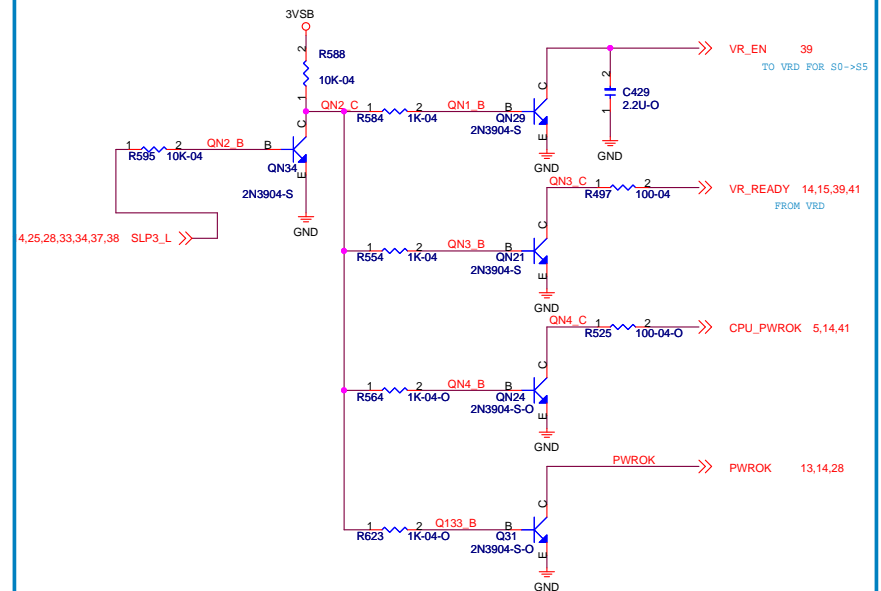
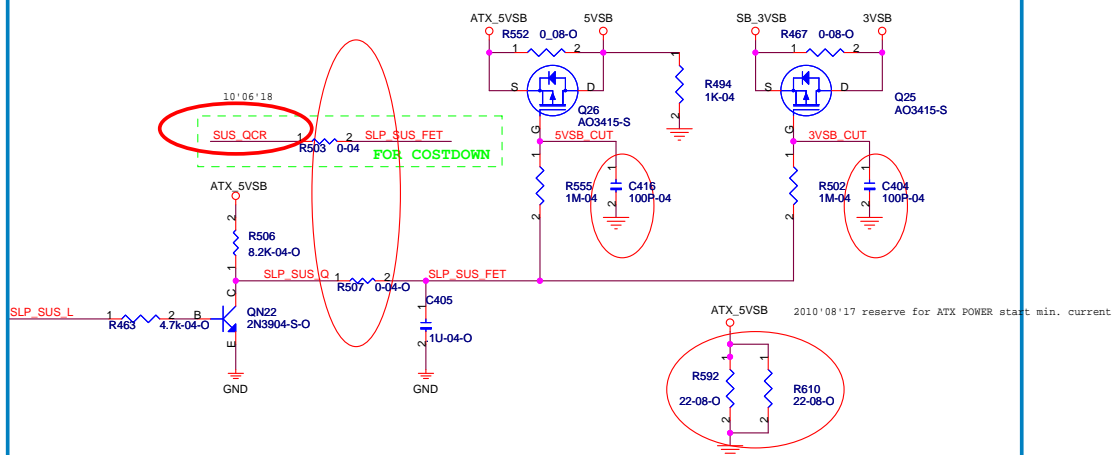
- 1)AC ON: 3VSB vs RSMRST(t204: min 10ms)
- 2)AC OFF: 3VSB>2.9V when RSMRST<0.8V

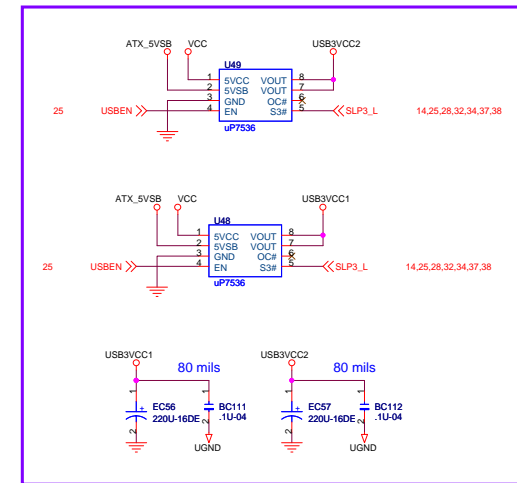
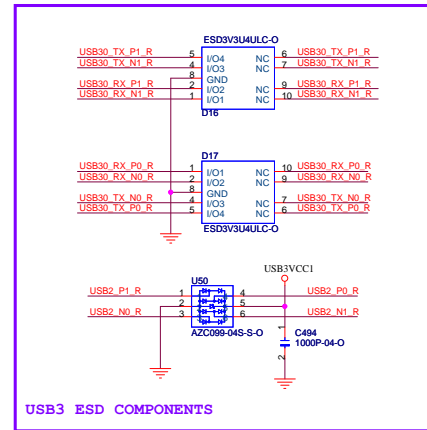
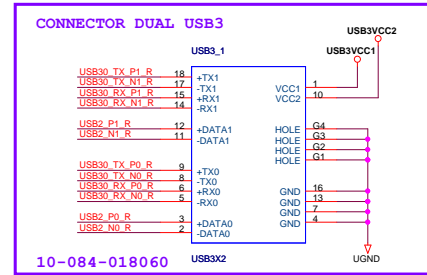
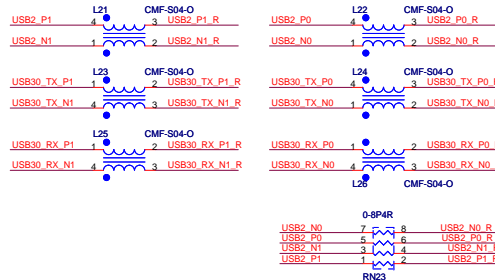
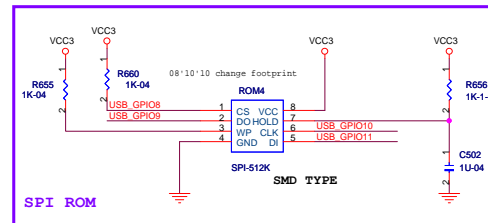
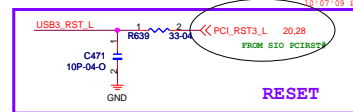
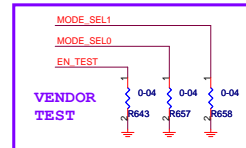
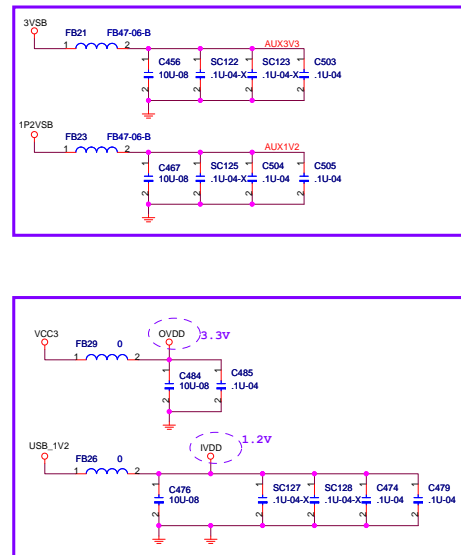
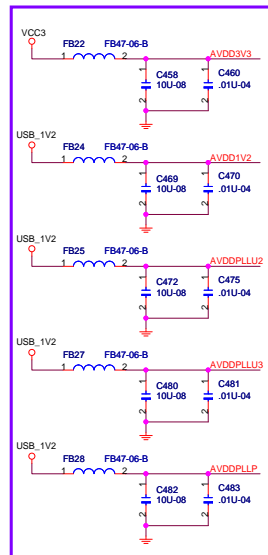
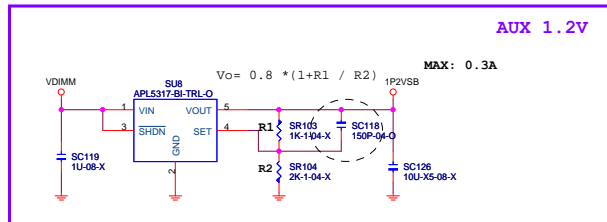
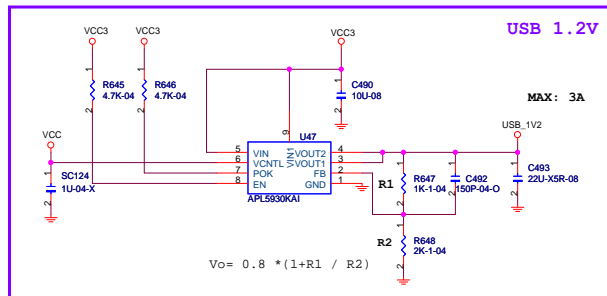
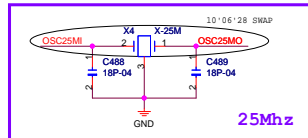
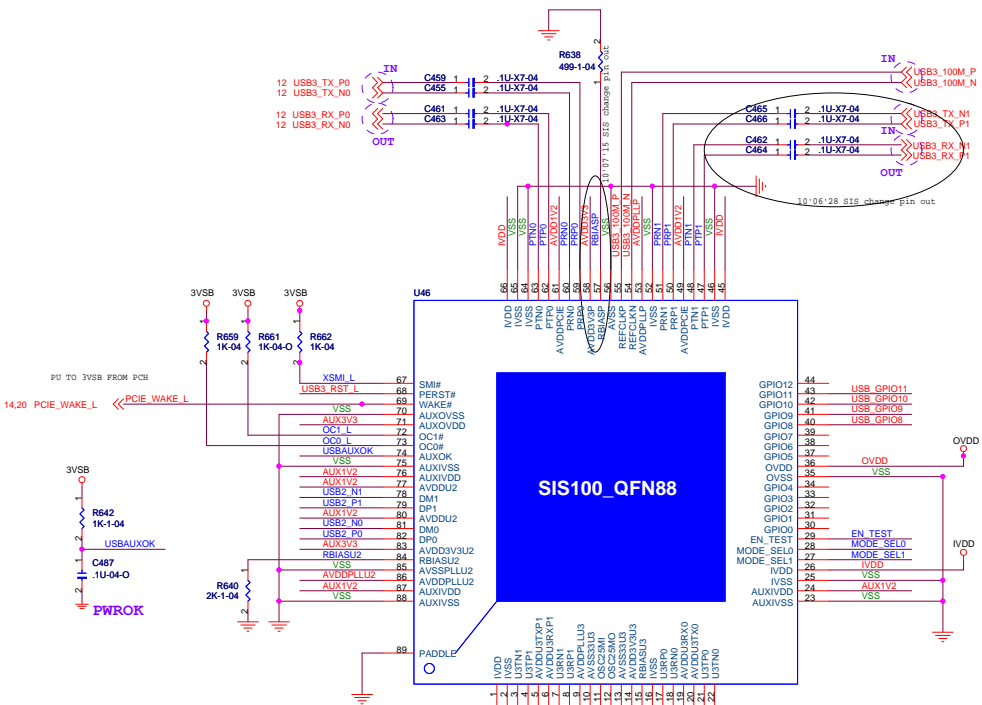


FOR COSTDOWN



10'06'18



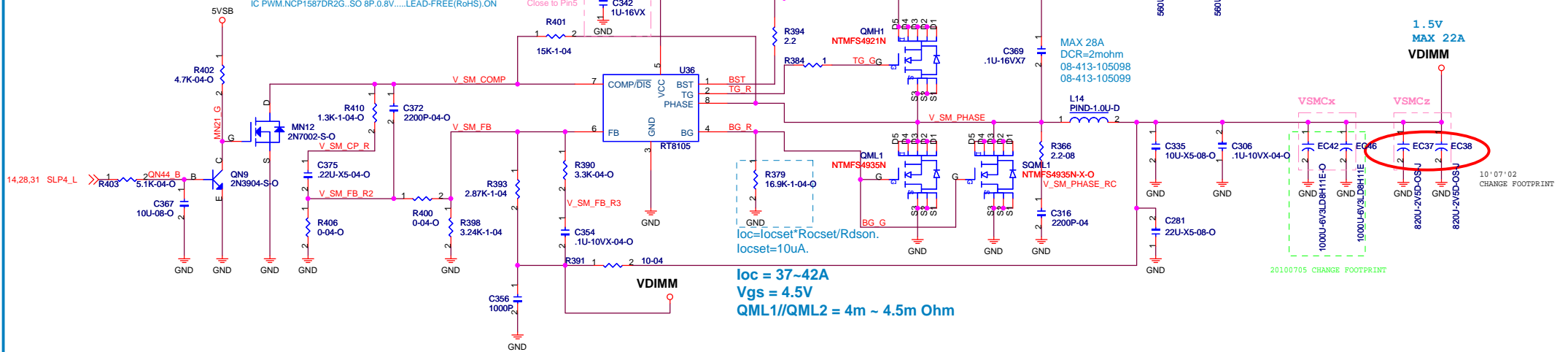


VD IMM

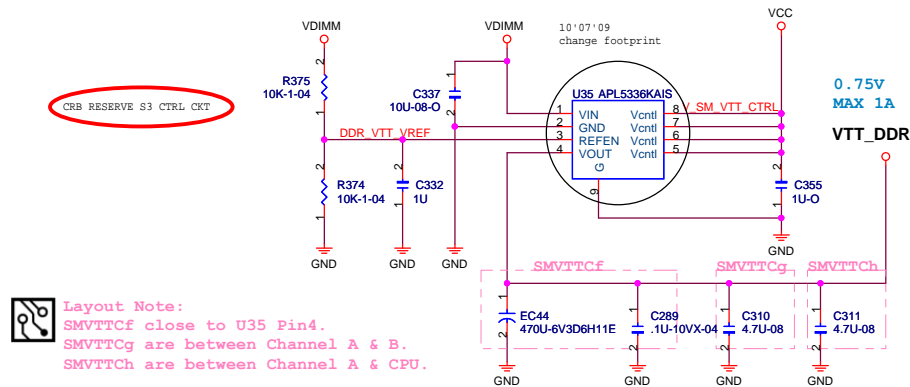
SLP4_L	High	Low
NCP1587DR2G	Enable	Disable

NCP1587 & RT8116 pin to pin.
RT8116: boot voltage 30V.

02-436-587890
IC PWM.NCP1587DR2G..SO 8P.0.8V.....LEAD-FREE(RoHS).ON

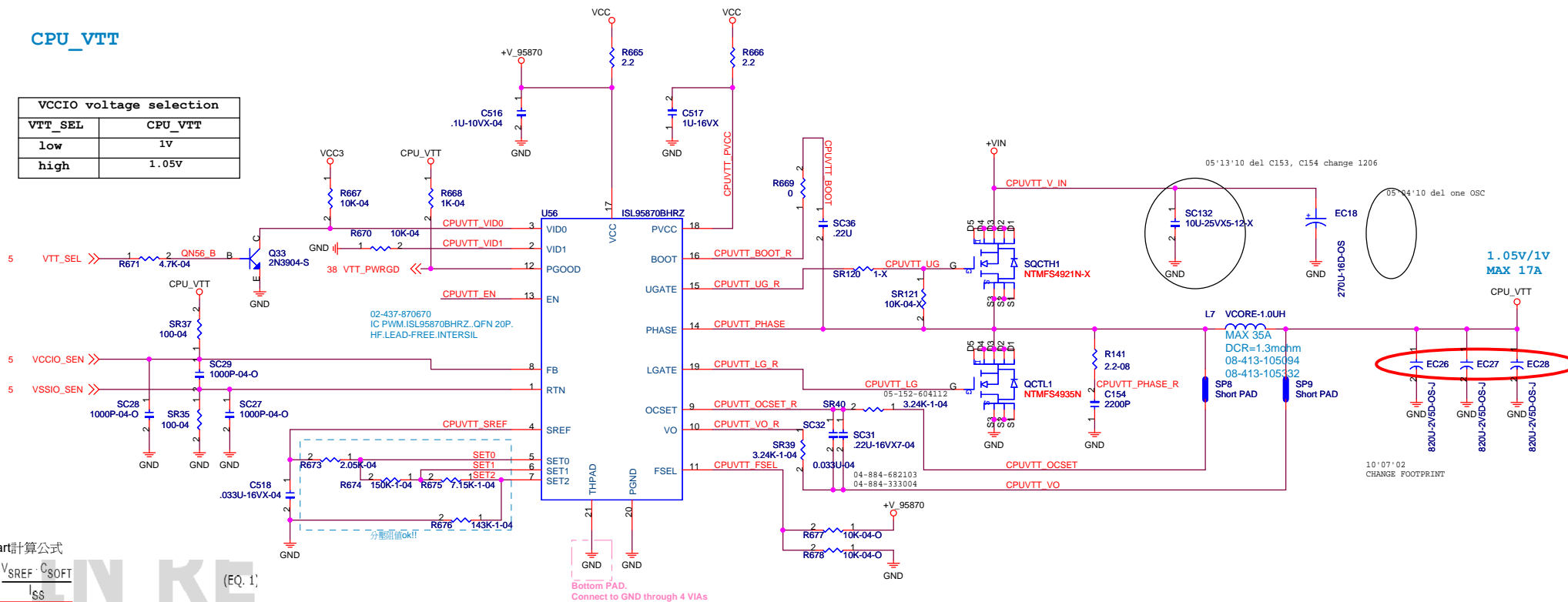


DDR_VTT



CPU_VTT

VCCIO voltage selection	
VTT_SEL	CPU_VTT
low	1V
high	1.05V



Soft-start計算公式

$$t_{SS} = \frac{V_{SREF} \cdot C_{SOFT}}{I_{SS}} \quad (EQ. 1)$$

Where:

- I_{SS} is the soft-start current source at the 20μA limit
- V_{SREF} is the buffered V_{REF} reference voltage

Vout計算公式

TABLE 2. ISL95870B VID TRUTH TABLE

VID STATE		RESULT			
VID1	VID0	CLOSE	V _{SREF}	V _{OUT}	
1	1	SW0	V _{SET1}	V _{OUT1}	
1	0	SW1	V _{SET2}	V _{OUT2}	
0	1	SW2	V _{SET3}	V _{OUT3}	
0	0	SW3	V _{SET4}	V _{OUT4}	

Equations 21, 22, 23 and 24 give the specific V_{SET} equations for the ISL95870B setpoint reference voltages.

The ISL95870B V_{SET1} setpoint is written as Equation 21:

$$V_{SET1} = V_{REF} \quad (EQ. 21)$$

The ISL95870B V_{SET2} setpoint is written as Equation 22:

$$V_{SET2} = V_{REF} \cdot \left(1 + \frac{R_{SET1}}{R_{SET2} + R_{SET3} + R_{SET4}} \right) \quad (EQ. 22)$$

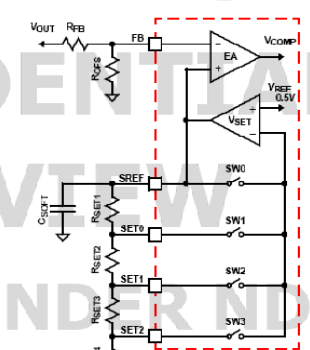
The ISL95870B V_{SET3} setpoint is written as Equation 23:

$$V_{SET3} = V_{REF} \cdot \left(1 + \frac{R_{SET1} + R_{SET2}}{R_{SET3} + R_{SET4}} \right) \quad (EQ. 23)$$

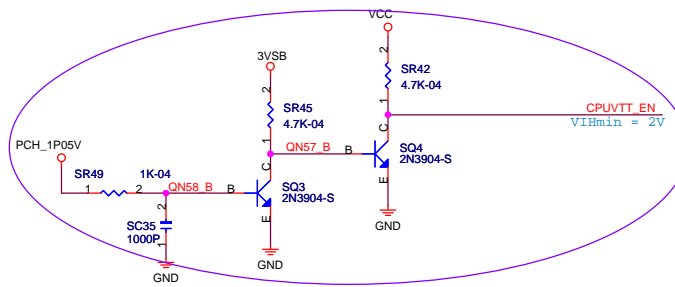
The ISL95870B V_{SET4} setpoint is written as Equation 24:

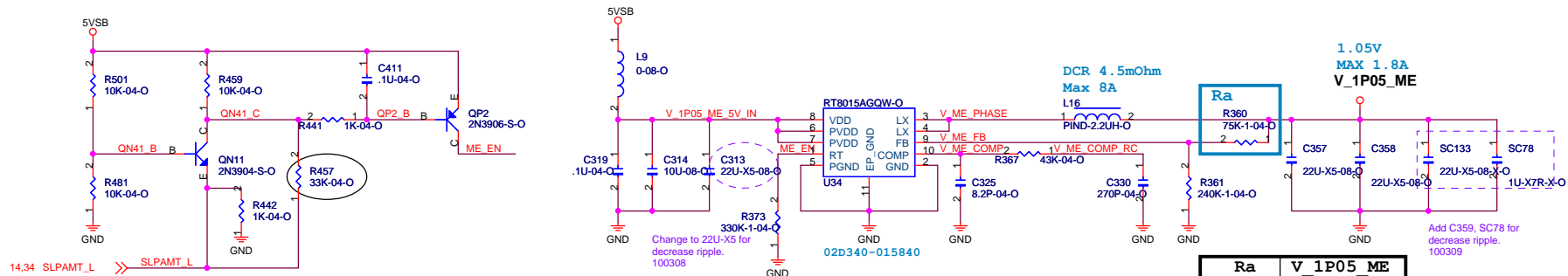
$$V_{SET4} = V_{REF} \cdot \left(1 + \frac{R_{SET1} + R_{SET2} + R_{SET3}}{R_{SET4}} \right) \quad (EQ. 24)$$

FIGURE 10. ISL95870B VOLTAGE PROGRAMMING CIRCUIT



Frequency selection	
F (Hz)	FSEL
300K	Directly to GND
500K	Floating
600K	100K ohm to GND
1M	Pull-up to VCC

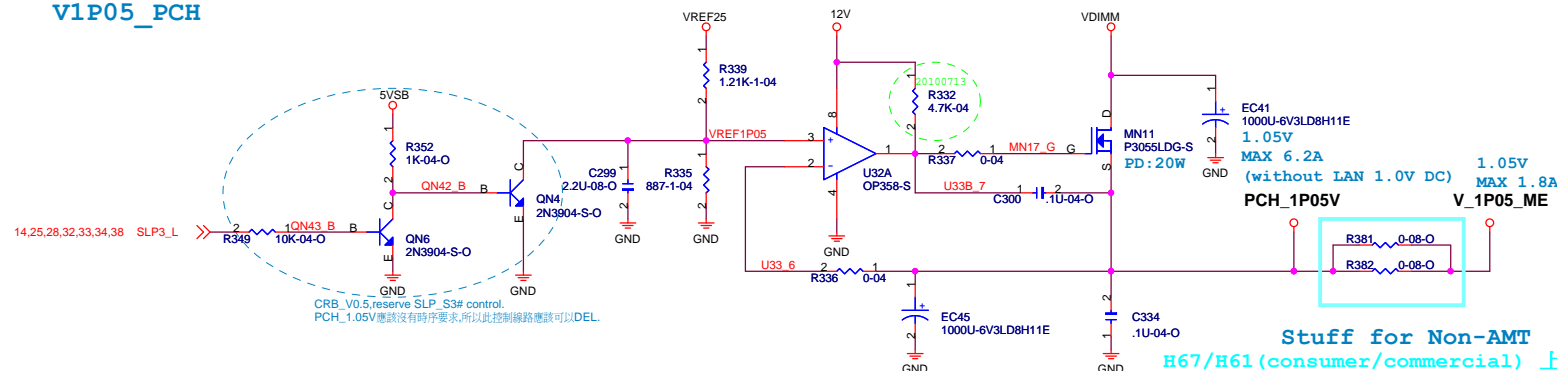




V1P05_ME

Q67/Q65 上件

V1P05_PCH



BOM Note:

02-340-015840..._dn10_r8106a
IC REG.RT8015AGQW.WDFN 10P.3A.LEAD-FREE(RoHS/HF).
RICHTER

08-413-225094...choke_2r2m_pt4d9x4d6mm
POWER IND.2.2uH.20%.8A.4.5m OHM.DIP 2P.8.2*8.2*7.5*6.7
mm.AKL0806MN-2R2M-L3.2....LEAD-FREE(RoHS).MAGIC

05-152-750113
RES.75K.1/16W.1%.SMD 0402....LEAD-FREE(RoHS/HF).

05-152-430103
RES.43K.1/16W.5%.SMD 0402....LEAD-FREE(RoHS/HF).

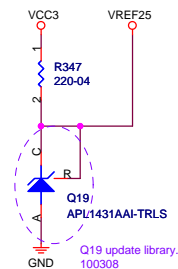
05-152-240114
RES.240K.1/16W.1%.SMD 0402....LEAD-FREE(RoHS/HF).

04-880-828100
C/C.8.2pF.50V.0.25pL..NPO...SMD 0402....LEAD-FREE(RoHS/HF).

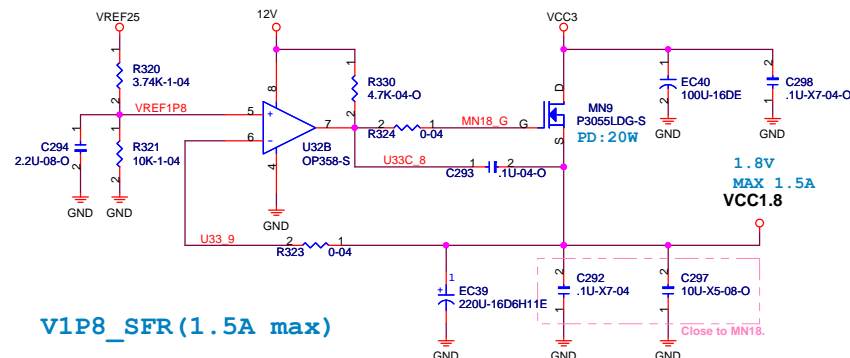
Stuff for Non-AMT

H67/H61 (consumer/commercial) 上件

VREF25



V1P8_SFR (1.5A max)



Elitegroup Computer Systems

DC/DC V1P05_PCH,ME/V1P8_SFR

Document Number
Q67/ Q65/ H67/ H61 H2-AD

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★

Stuff VSAGz

VCCSA voltage selection	
VID	+V SA
0	0.925V
1	0.85V

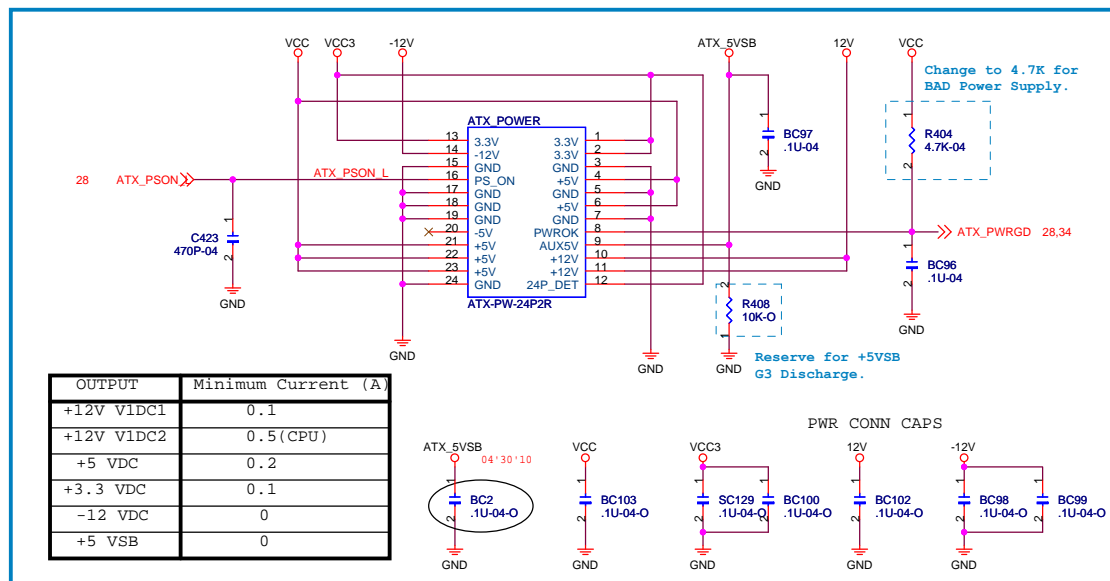
Stuﬀ VSAGz

VCCSA voltage selection	
VID	+V _{SA}
0	0.925V
1	0.85V

*

VCCSA voltage selection	
Rf	+V_SA
unstuff	0.85V
stuff	0.925V

Rf	+V_{SA}
unstuffed	0.85V
stuff	0.925V



OUTPUT	Minimum Current (A)
+12V V1DC1	0.1
+12V V1DC2	0.5(CPU)
+5 VDC	0.2
+3.3 VDC	0.1
-12 VDC	0
+5 VSB	0

ATX Power 24PIN

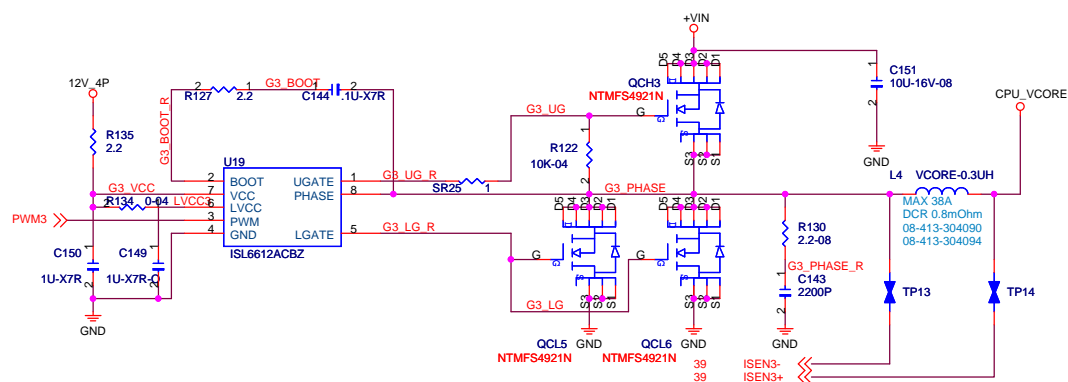
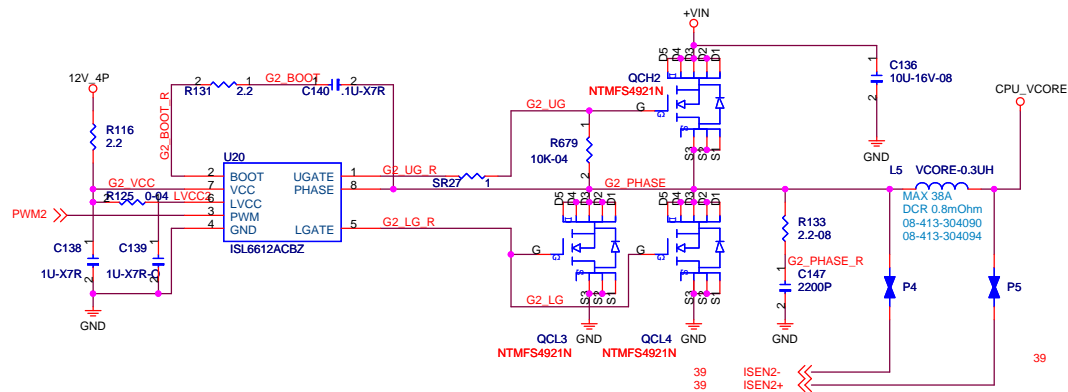
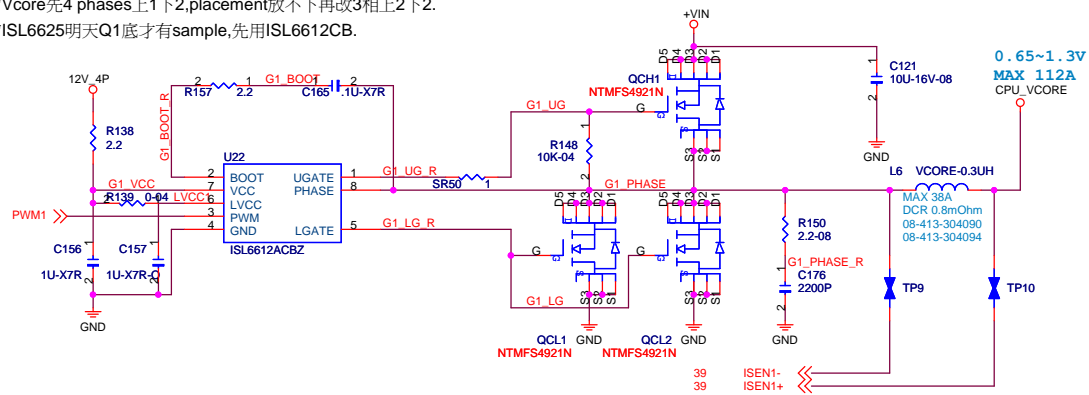
[illegible]

2010'08'19 reserve for ATX POWER start min. current

**Vcore先4 phases上1下2,placement放不下再改3相上2下2.

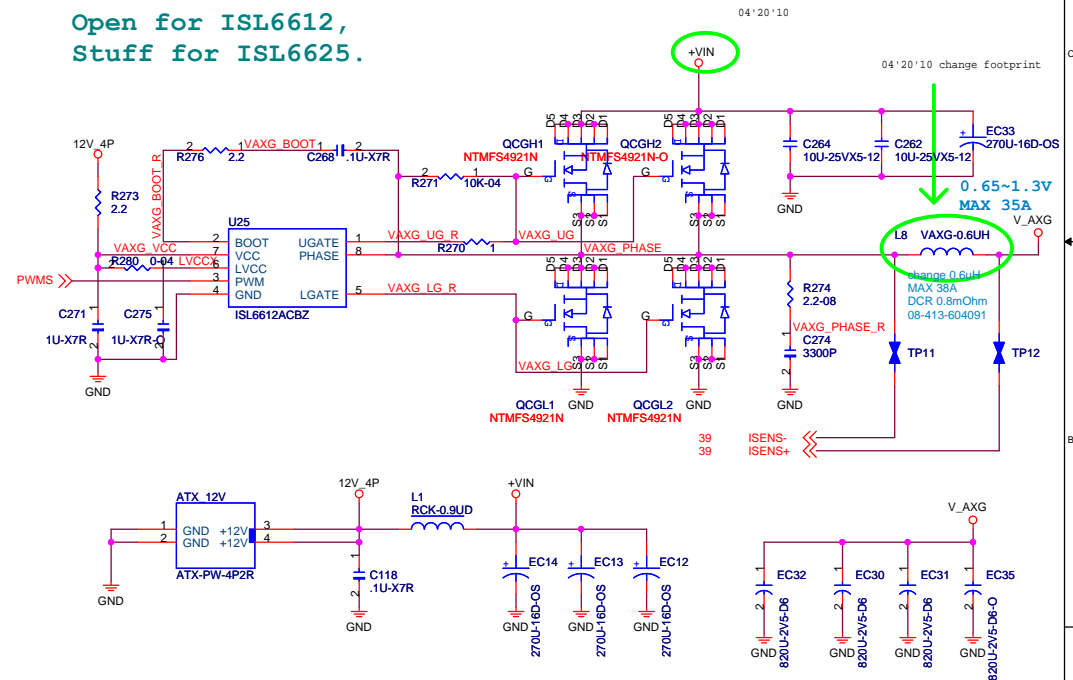
**ISL6625明天Q1底才有sample,先用ISL6612CB.

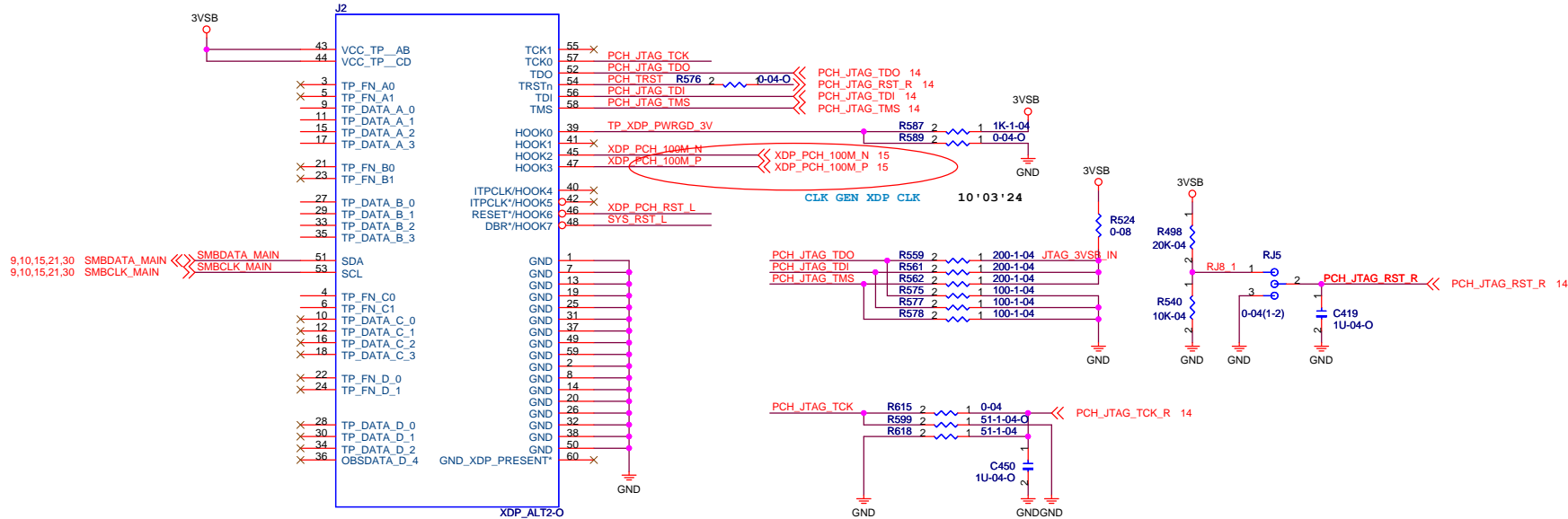
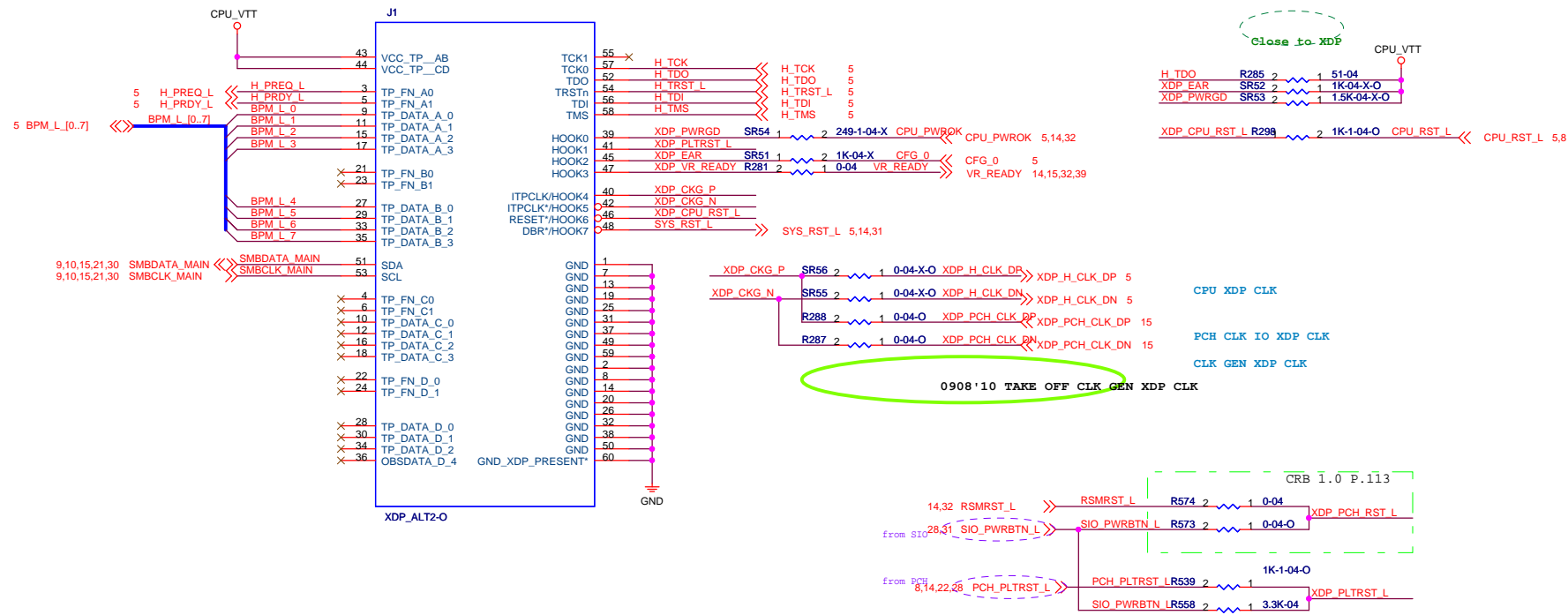
02-415-612672
IC DRIVER:ISL6612ACBZ..SO 8P,LEAD-FREE,INTERSIL



Stuff for ISL6612,
Open for ISL6625.

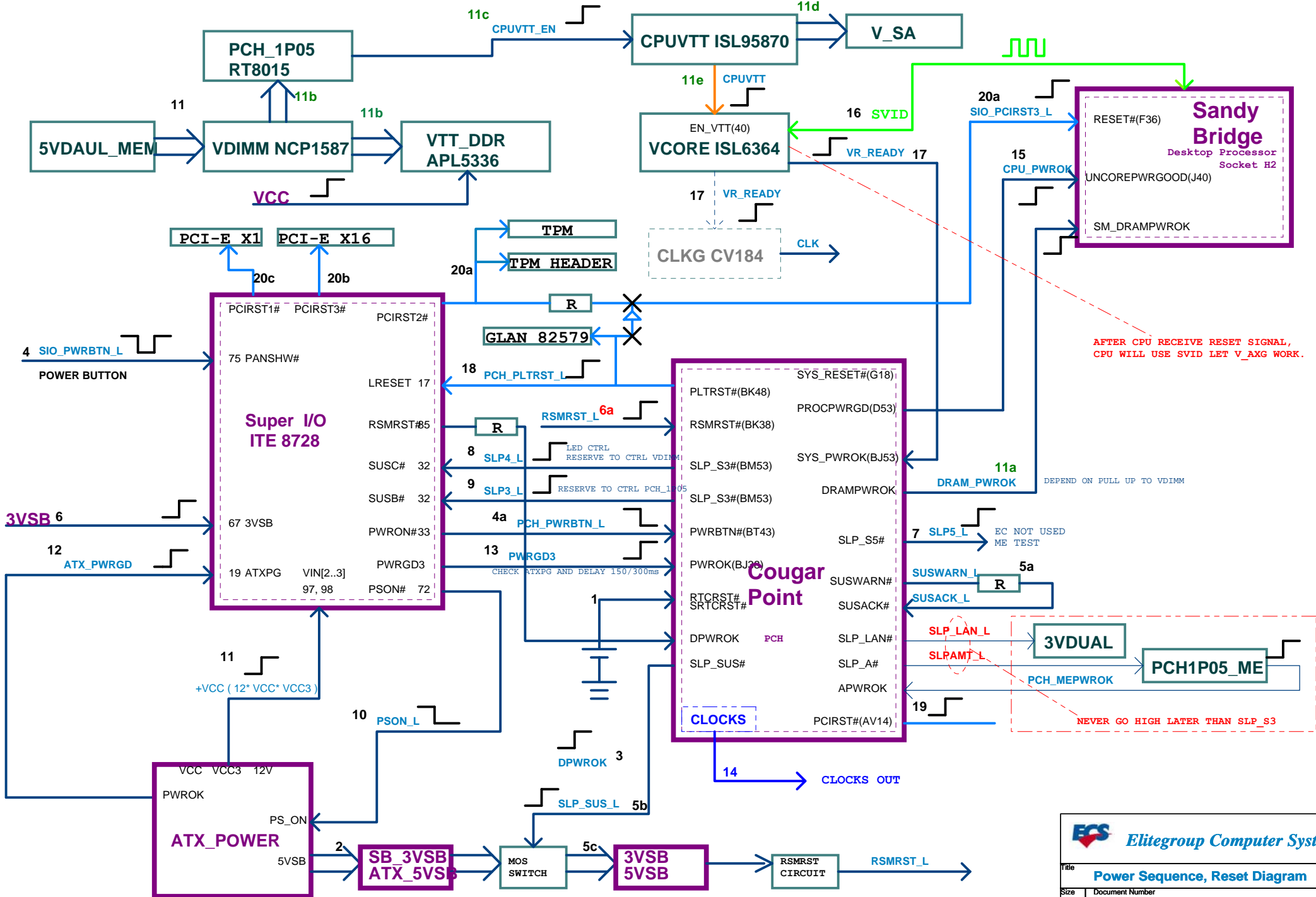
Open for ISL6612,
Stuff for ISL6625.





DESIGN NOTE:
PCH JTAG

DESIGN NOTE:
DEFENSIVE DESIGN



AFTER CPU RECEIVE RESET SIGNAL, CPU WILL USE SVID LET V_AXG WORK.

DEPEND ON PULL UP TO VDIMM

EC NOT USED ME TEST

NEVER GO HIGH LATER THAN SLP_S3

NOTE:

Sugar Bay Platform has two clock mode:

1.Integrated Clock Mode (Generate by PCH)

2.Buffer Through Mode (Generate by Clock Gen.)

If we choose Integrated Clock Mode, we should unstuff Clock Gen. circuit.

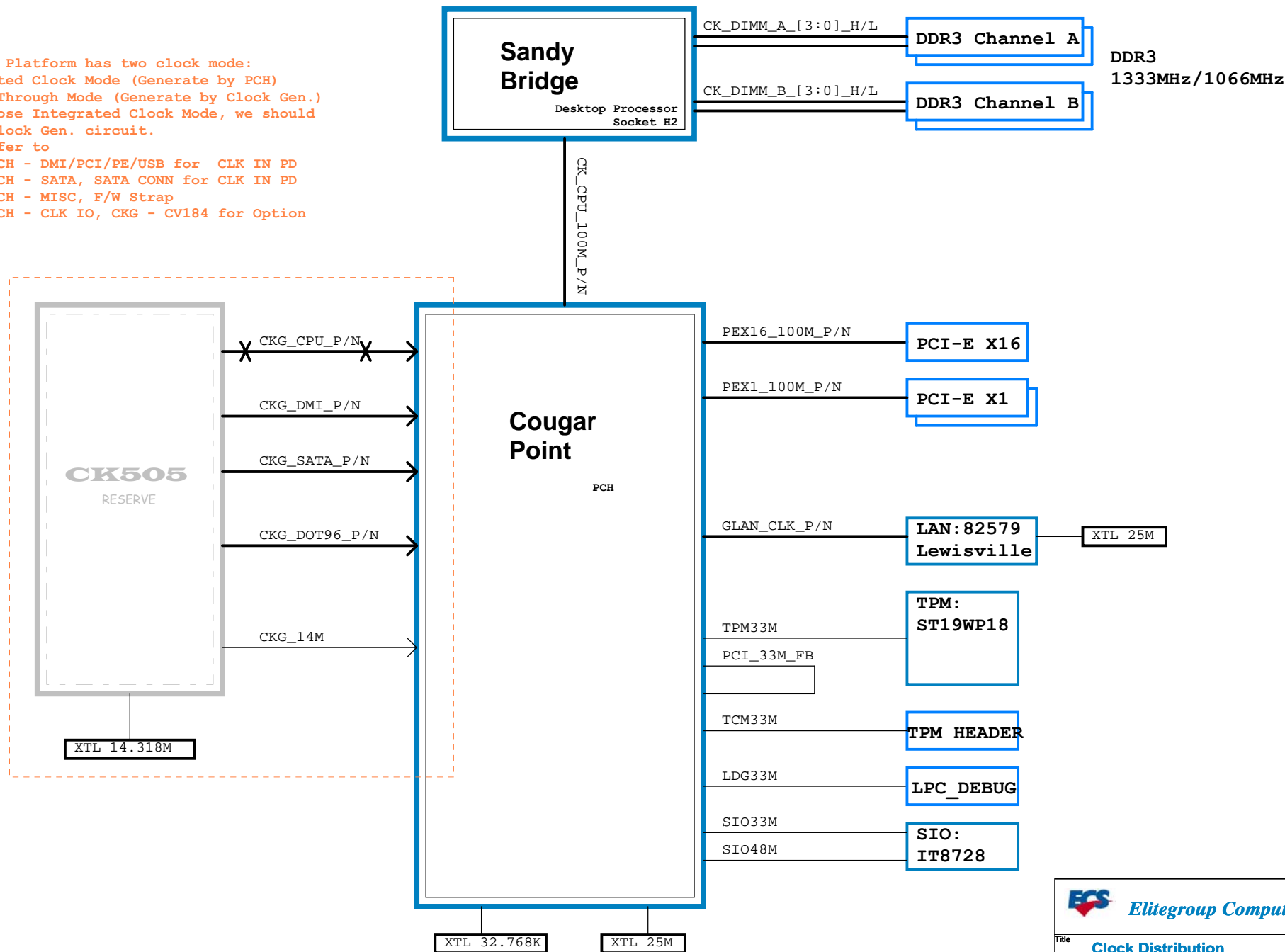
Please refer to

Page.12 PCH - DMI/PCI/PE/USB for CLK IN PD

Page.13 PCH - SATA, SATA CONN for CLK IN PD

Page.14 PCH - MISC, F/W Strap

Page.15 PCH - CLK IO, CKG - CV184 for Option



Elitegroup Computer Systems

Title
Clock Distribution

Size Custom Document Number
Q67/ Q65/ H67/ H61 H2-AD

Rev
V1.0

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