



H61H2-LM3

Rev : 1.0

ECS
CONFIDENTIAL

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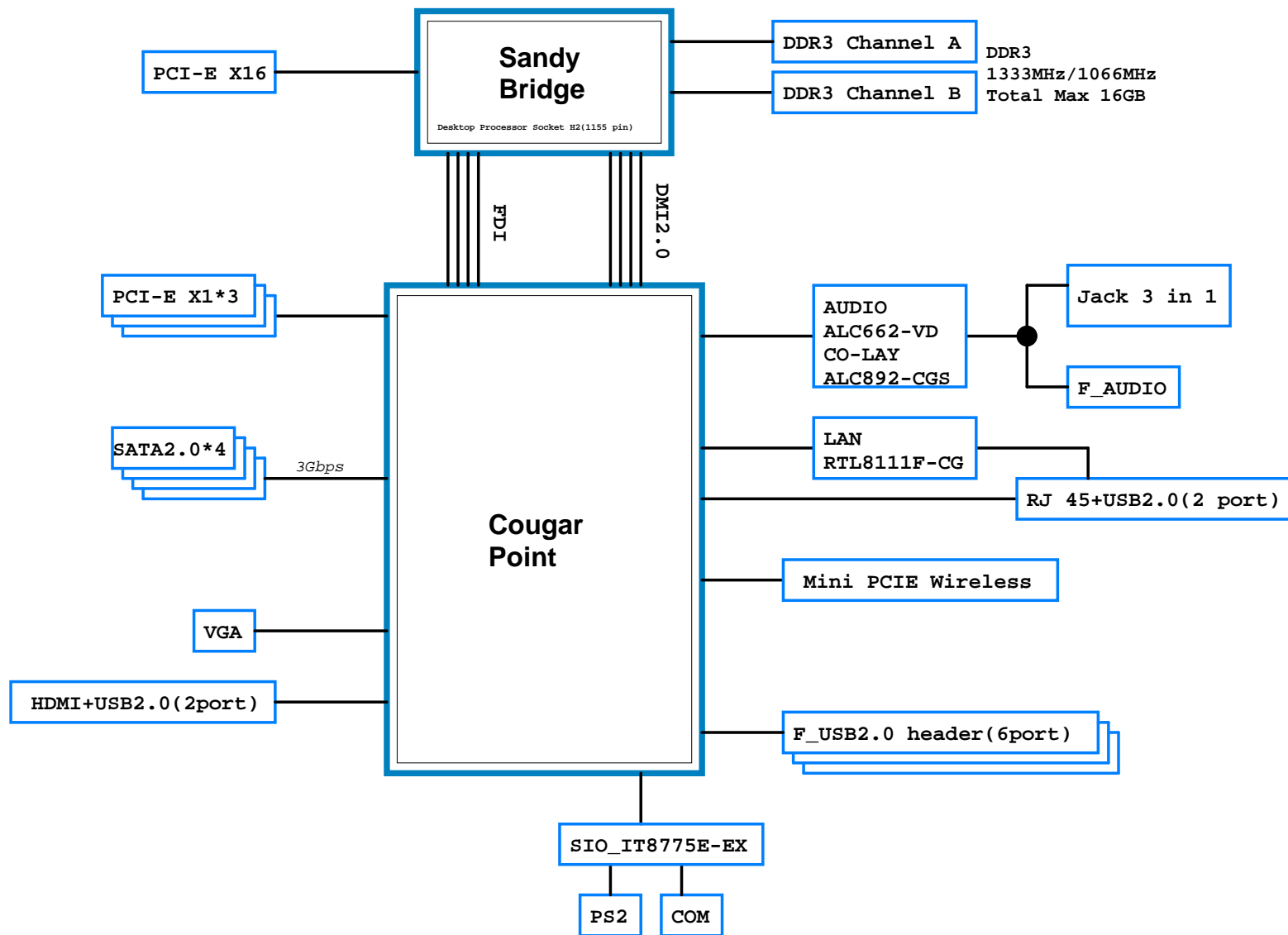
REVISION HISTORY:

Rev	Date	Notes
V0.1	11/06/29	
V0.2	11/07/29	1.CLK SI:R374=51 OHM,R376=51 OHM,R378=47 OHM,R425=47 OHM 2.VGA SI:R27=47 OHM,R28=47 OHM,R18=120 OHM,R20=120 OHM 3.DC SI:PFB3=0 OHM,ADD C289,DEL SC75 4.SPEC CHANGE:DEL USB_HDMI,ADD HDMI,ADD USBX2 5.COLAY ALC662-VC:ADD R102,EC88,U18,MN14,R781,D16,R780,R537,R542,R543 6.HDA SI:ADD R112 7.ADD DPWROK CIRCUIT:ADD R680,C656,MN15,R660,QN12,R646 8.ADD WIFI LED CIRCUIT:ADD D51,R655 9.VRM12 CHANGE:C463=470P,C231=2200P,C230=1500P,R254=6.49K,R272=11.5K,R162=3.01K, C240=1000P,C454=3300P,R294=93.1K 10.VRM 65W: R275=29.4K,R300=21.5K,R217=60.4K DEL:R225,C2220,R255,R217,R319,R898,R157,C159,R159,R148,C163,R149,R186,C119 C118,R167,C171,L5,QCH4,QCL4,QCL8 ADD:R229,R279,R370 11.WIFI LED:ADD D51,R655,C659

NOTE:

Design by
428971_Sugar Bay_PDQ_Rev2.0
443554_Intel_6_Series_C200_Series_Chipset_EDS_rev2_1
428969_Sugar Bay_CRB_Rev1.1

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PCH-GPIO function


Pin Name	Power Well	Usage	Default Status
GPIO1	VCC3	GP1_BOMDET2	GPI
GPIO6	VCC3	GP6_BOMDET3	GPI
GPIO7	VCC3	GP7_BOMDET4	GPI
GPIO9	3VSB	WIFI_CTL	Native
GPIO10	3VSB	USB_OC_L6	Native
GPIO11	3VSB	SMBALERT_L	Native
GPIO12	3VSB	MODE_TRIGGER	Native
GPIO13	3VSB	LPC_PME	GPI
GPIO14	+DIMM_5VDUAL	PCH_LED1	Native
GPIO17	VCC3	GP17_BOMDET1	GPI
GPIO21	VCC3	GPIO21_COM2_DET	GPI
GPIO22	VCC3	CLR_CMOS_GP22	GPI
GPIO23	VCC3	LPC_DRQ1_L	Native
GPIO24	3VSB	PCH_SKTOCC_L	GPO
GPIO27	+PS_3VSB	MS_GP0	GPI
GPIO30	+PS_3VSB	SUSWARN_L	Native
GPIO31	+PS_3VSB	MS_GP1	GPI
GPIO39	VCC3	GPIO39_CASE0	GPI
GPIO40	3VSB	USB_OC_L1	Native
GPIO41	3VSB	USB_OC_L2	Native
GPIO42	3VSB	USB_OC_L3	Native
GPIO43	3VSB	USB_OC_L4	Native
GPIO45	3VSB	WLAN_DIS_L	Native
GPIO48	VCC3	GPIO48_CASE1	GPI
GPIO57	3VSB	MODE_CTRL	GPI
GPIO59	3VSB	USB_OC_L0	Native
GPIO63	3VSB	SLP5_L	Native
GPIO64	VCC3	LDG33M	Native
GPIO67	VCC3	SIO48M	Native
GPIO72	3VSB	GPIO72_BOMDET5	Native

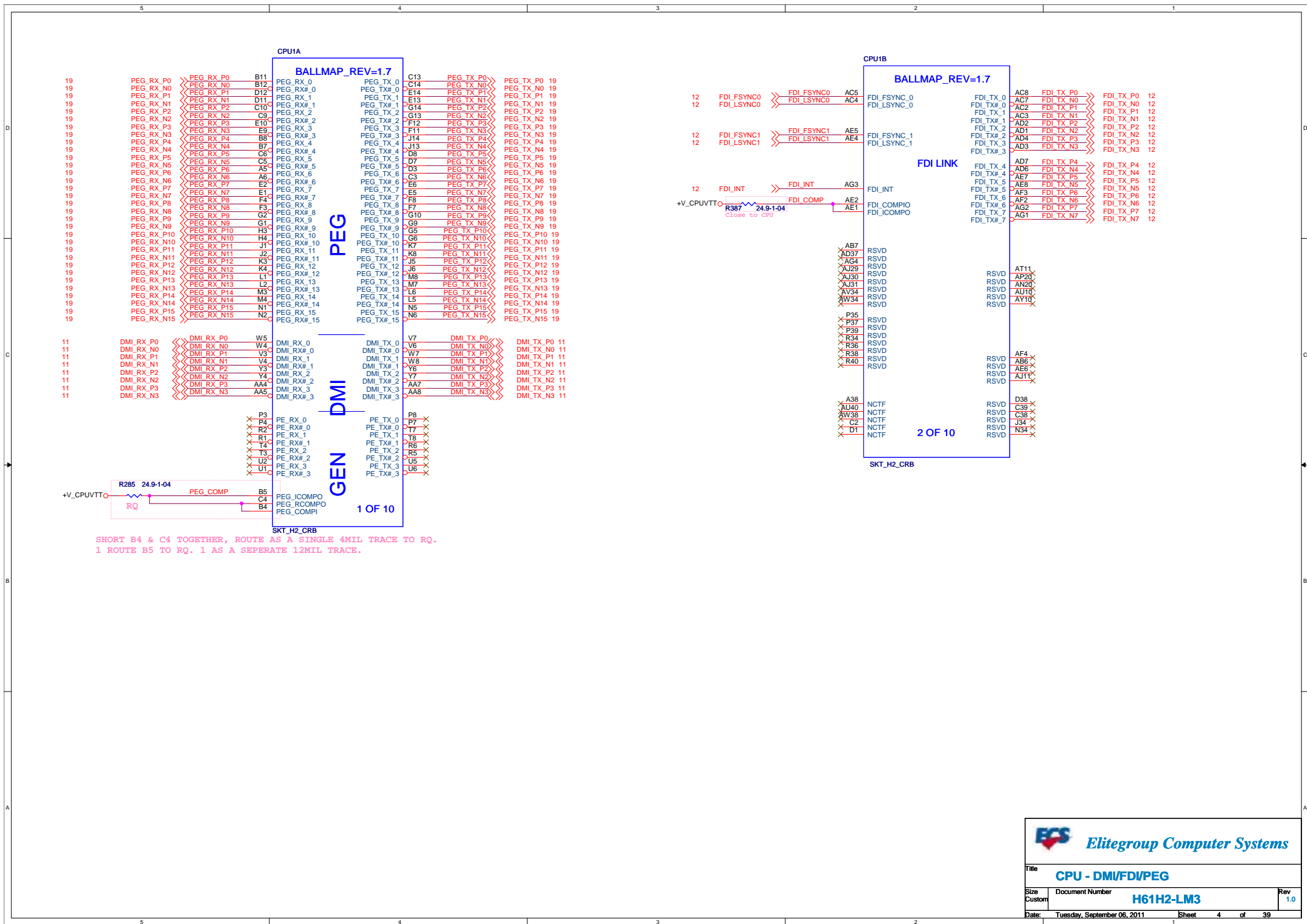
SIO-GPIO function

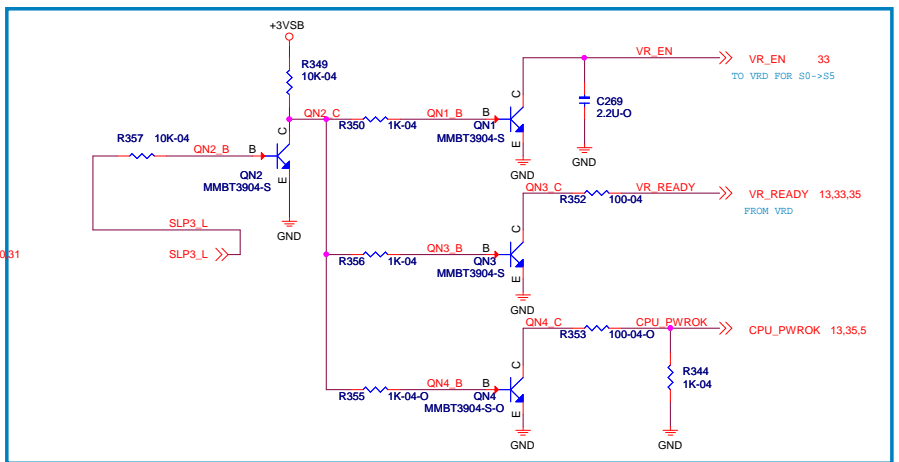
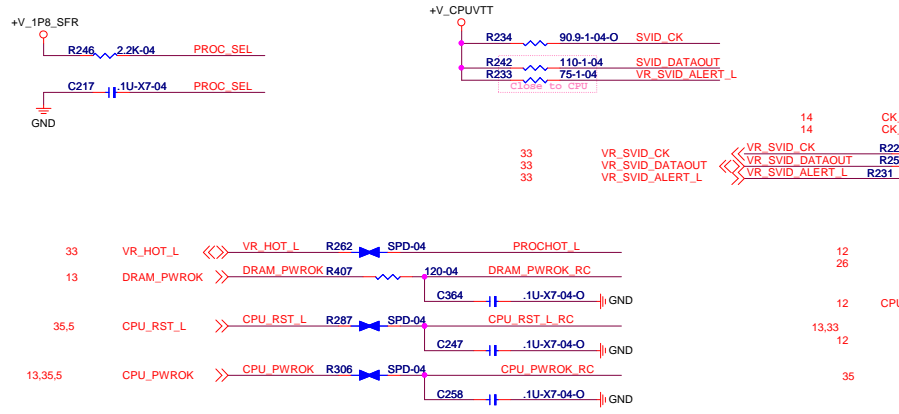
Pin Name	Power Well	Usage	Default Status
GP10	3VSB	SIO_PCIRST3_L	PCIRST3#
GP12	VCC3	SIO_PCIRST1_L	PCIRST1#
GP22	3VSB	SIO_LED0	GP22
GP23	3VSB	DPWROK	DPWROK
GP30	VCC3	ATXPWRGD	ATXPWRGD
GP31	VCC3	CTS1_L	CTS1#
GP32	VCC3	SIO_RI1_L	RI1#
GP33	VCC3	DCD1_L	DCD1#
GP36	VCC3	FAN_CTL3	FAN_CTL3
GP37	VCC3	FAN_TAC3	FAN_TAC3
GP40	3VSB	GPIO40_S4S5	3VSB5W#
GP41	3VSB	SIN1	SIN1
GP42	3VSB	PSO_N_L	PSO_N#
GP43	3VSB	FP_PWRBTN_L	PANSWH#
GP44	3VSB	SIO_PWRBTN_L	PWRON#
GP45	VCC3	DSR1_L	DSR1#
GP51	VCC3	FAN_CTL2	FAN_CTL2
GP52	VCC3	FAN_TAC2	FAN_TAC2
GP53	3VSB	SLP4_L	SUSC#
GP54	3VSB	LPC_PME_L	PME#
GP55	3VSB	RSMRST_L	RSMRST#
GP56	3VSB	MCLK	MCLK
GP57	3VSB	MDATA	MDAT
GP60	3VSB	KCLK	KCLK
GP61	3VSB	KDATA	KDAT
GP62	VCC3	KBRST_L	KRST#

H61 fuction PCI INT#

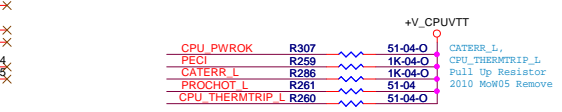
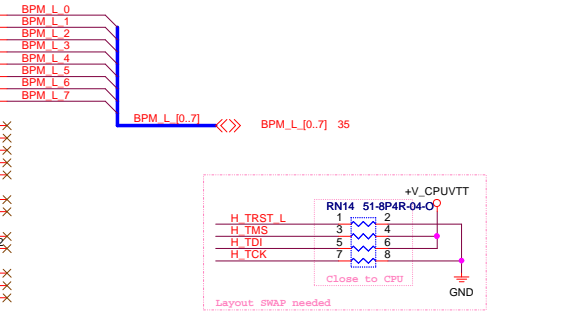
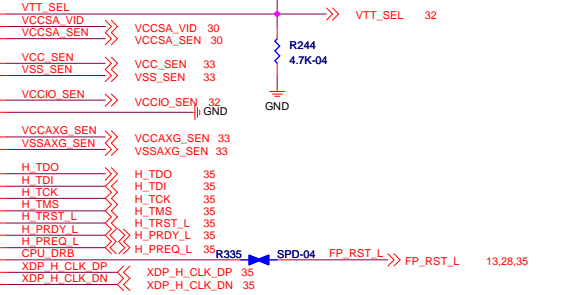
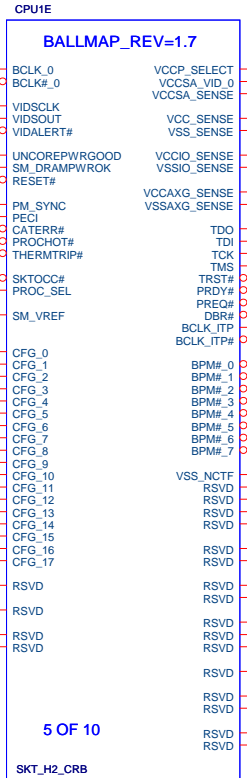
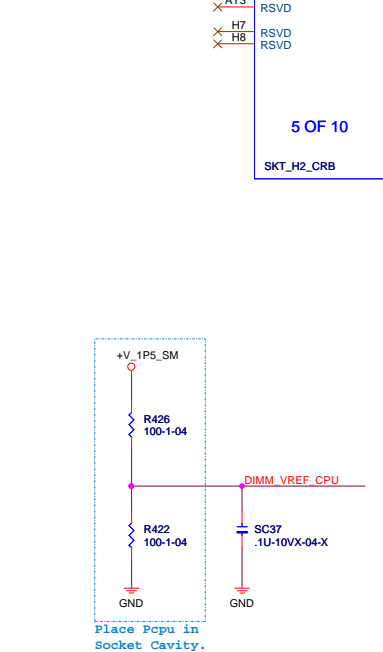
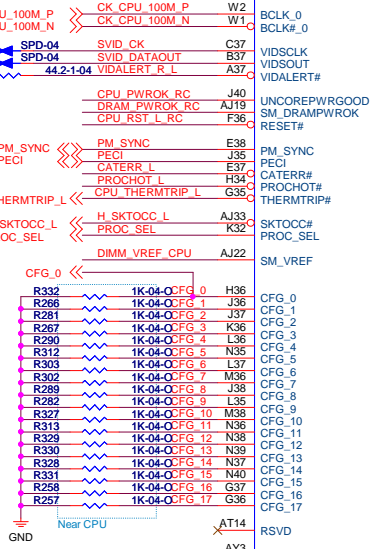
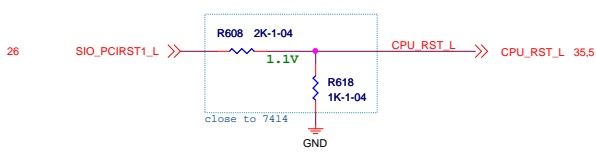
Function	INT PORT	PCIE 1X PORT	Chipset
LAN Controller	INT A#	PE_TX/RX_5	RTL8111F
PCIE1X_4 Wireless Card	INT C#	PE_TX/RX_3	H61 integrated
PCIE1X_1 Slot	INT D#	PE_TX/RX_4	H61 integrated
PCIE1X_2 Slot	INT B#	PE_TX/RX_6	H61 integrated
PCIE1X_3 Slot	INT B#	PE_TX/RX_2	H61 integrated
SATA Controller	INT B#	NA	H61 integrated

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Power Down Sequencing Circuit



CFG	H	L	DESCRIPTION
0	reserved	reserved	reserved
1	reserved	reserved	reserved
2	NORMAL	REVERSE	PEGLANE REVERSAL[0], X16
3	reserved	reserved	reserved
4	reserved	reserved	reserved
5	*	*	PEOFGSEL[0]
6	*	*	PEOFGSEL[1]
7	reserved	reserved	reserved
8	reserved	reserved	reserved
9	reserved	reserved	reserved
10	reserved	reserved	reserved
11	reserved	reserved	reserved
12	reserved	reserved	reserved
13	reserved	reserved	reserved
14	reserved	reserved	reserved
15	reserved	reserved	reserved

CFG[0..17] HAVE INTERNAL PULL-UPS

PCIE CONFIG	SEL0	SEL1	CFG[5:6]
1 X 16	1	1	01=2X8,
2 X 8	0	1	10=RESERVED,
			00=X8,X4,X4

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9	M_DATA_A[0..63]	← M_DATA_A[0..63]
9	M_DQS_A_P[0..7]	← M_DQS_A_P[0..7]
9	M_DQS_A_N[0..7]	← M_DQS_A_N[0..7]
9	M_MA_A[0..15]	← M_MA_A[0..15]
9	M_BS_A[0..2]	← M_BS_A[0..2]
9	M_CS_A_L[0..1]	← M_CS_A_L[0..1]
9	M_CKE_A[0..1]	← M_CKE_A[0..1]
9	M_ODT_A[0..1]	← M_ODT_A[0..1]
9	M_CLK_A_P[0..1]	← M_CLK_A_P[0..1]
9	M_CLK_A_N[0..1]	← M_CLK_A_N[0..1]
9	M_WE_A_L	← M_WE_A_L
9	M_CAS_A_L	← M_CAS_A_L
9	M_RAS_A_L	← M_RAS_A_L

DDR3 CH.A

DDR3_DRAMRST_L ← DDR3_DRAMRST_L

9	M_DATA_B[0..63]	← M_DATA_B[0..63]
9	M_DQS_B_P[0..7]	← M_DQS_B_P[0..7]
9	M_DQS_B_N[0..7]	← M_DQS_B_N[0..7]
9	M_MA_B[0..15]	← M_MA_B[0..15]
9	M_BS_B[0..2]	← M_BS_B[0..2]
9	M_CS_B_L[0..1]	← M_CS_B_L[0..1]
9	M_CKE_B[0..1]	← M_CKE_B[0..1]
9	M_ODT_B[0..1]	← M_ODT_B[0..1]
9	M_CLK_B_P[0..1]	← M_CLK_B_P[0..1]
9	M_CLK_B_N[0..1]	← M_CLK_B_N[0..1]
9	M_WE_B_L	← M_WE_B_L
9	M_CAS_B_L	← M_CAS_B_L
9	M_RAS_B_L	← M_RAS_B_L

DDR3 CH.B

M_DATA_A0	AJ3	SA_DQ_0
M_DATA_A1	AJ4	SA_DQ_1
M_DATA_A2	AL3	SA_DQ_2
M_DATA_A3	AL4	SA_DQ_3
M_DATA_A4	AJ2	SA_DQ_4
M_DATA_A5	AJ1	SA_DQ_5
M_DATA_A6	AL2	SA_DQ_6
M_DATA_A7	AL1	SA_DQ_7
M_DATA_A8	AN1	SA_DQ_8
M_DATA_A9	AN4	SA_DQ_9
M_DATA_A10	AR3	SA_DQ_10
M_DATA_A11	AR4	SA_DQ_11
M_DATA_A12	AN2	SA_DQ_12
M_DATA_A13	AN3	SA_DQ_13
M_DATA_A14	AR2	SA_DQ_14
M_DATA_A15	AR1	SA_DQ_15
M_DATA_A16	AW2	SA_DQ_16
M_DATA_A17	AW3	SA_DQ_17
M_DATA_A18	AV5	SA_DQ_18
M_DATA_A19	AW5	SA_DQ_19
M_DATA_A20	AU2	SA_DQ_20
M_DATA_A21	AU3	SA_DQ_21
M_DATA_A22	AU5	SA_DQ_22
M_DATA_A23	AV5	SA_DQ_23
M_DATA_A24	AV7	SA_DQ_24
M_DATA_A25	AU7	SA_DQ_25
M_DATA_A26	AV9	SA_DQ_26
M_DATA_A27	AU9	SA_DQ_27
M_DATA_A28	AV7	SA_DQ_28
M_DATA_A29	AW7	SA_DQ_29
M_DATA_A30	AW9	SA_DQ_30
M_DATA_A31	AU9	SA_DQ_31
M_DATA_A32	AU35	SA_DQ_32
M_DATA_A33	AW37	SA_DQ_33
M_DATA_A34	AU39	SA_DQ_34
M_DATA_A35	AU36	SA_DQ_35
M_DATA_A36	AW35	SA_DQ_36
M_DATA_A37	AU36	SA_DQ_37
M_DATA_A38	AU38	SA_DQ_38
M_DATA_A39	AU37	SA_DQ_39
M_DATA_A40	AR40	SA_DQ_40
M_DATA_A41	AR37	SA_DQ_41
M_DATA_A42	AN38	SA_DQ_42
M_DATA_A43	AN37	SA_DQ_43
M_DATA_A44	AR39	SA_DQ_44
M_DATA_A45	AR38	SA_DQ_45
M_DATA_A46	AN39	SA_DQ_46
M_DATA_A47	AN40	SA_DQ_47
M_DATA_A48	AL40	SA_DQ_48
M_DATA_A49	AL37	SA_DQ_49
M_DATA_A50	AJ38	SA_DQ_50
M_DATA_A51	AJ37	SA_DQ_51
M_DATA_A52	AL39	SA_DQ_52
M_DATA_A53	AL38	SA_DQ_53
M_DATA_A54	AJ39	SA_DQ_54
M_DATA_A55	AJ40	SA_DQ_55
M_DATA_A56	AG40	SA_DQ_56
M_DATA_A57	AG37	SA_DQ_57
M_DATA_A58	AE38	SA_DQ_58
M_DATA_A59	AE37	SA_DQ_59
M_DATA_A60	AG39	SA_DQ_60
M_DATA_A61	AG38	SA_DQ_61
M_DATA_A62	AE39	SA_DQ_62
M_DATA_A63	AE40	SA_DQ_63

M_DQS_A_P0	AP3	SA_DQS_0
M_DQS_A_P1	AP3	SA_DQS_1
M_DQS_A_P2	AW4	SA_DQS_2
M_DQS_A_P3	AV8	SA_DQS_3
M_DQS_A_P4	AV37	SA_DQS_4
M_DQS_A_P5	AP38	SA_DQS_5
M_DQS_A_P6	AK38	SA_DQS_6
M_DQS_A_P7	AF38	SA_DQS_7

M_DQS_A_N0	AK2	SA_DQS#_0
M_DQS_A_N1	AP2	SA_DQS#_1
M_DQS_A_N2	AV4	SA_DQS#_2
M_DQS_A_N3	AW6	SA_DQS#_3
M_DQS_A_N4	AV36	SA_DQS#_4
M_DQS_A_N5	AP39	SA_DQS#_5
M_DQS_A_N6	AK39	SA_DQS#_6
M_DQS_A_N7	AF39	SA_DQS#_7

SKT_H2_CRB

BALLMAP_REV=1.7

SA_MA_0	AV27	M_MA_A0
SA_MA_1	AY24	M_MA_A1
SA_MA_2	AW24	M_MA_A2
SA_MA_3	AW23	M_MA_A3
SA_MA_4	AV23	M_MA_A4
SA_MA_5	AT24	M_MA_A5
SA_MA_6	AT23	M_MA_A6
SA_MA_7	AU22	M_MA_A7
SA_MA_8	AV22	M_MA_A8
SA_MA_9	AT22	M_MA_A9
SA_MA_10	AV28	M_MA_A10
SA_MA_11	AU21	M_MA_A11
SA_MA_12	AW32	M_MA_A12
SA_MA_13	AU20	M_MA_A13
SA_MA_14	AT20	M_MA_A14
SA_MA_15	AT20	M_MA_A15

SA_WE#_0	AW29	M_WE_A_L
SA_CAS#_0	AV30	M_CAS_A_L
SA_RAS#_0	AU28	M_RAS_A_L

SA_BS_0	AY29	M_BS_A0
SA_BS_1	AW28	M_BS_A1
SA_BS_2	AV20	M_BS_A2

SA_CS#_0	AU29	M_CS_A_L0
SA_CS#_1	AV32	M_CS_A_L1
SA_CS#_2	AW30	M_CS_A_L1
SA_CS#_3	AU33	M_CS_A_L1

SA_CKE_0	AV19	M_CKE_A0
SA_CKE_1	AT19	M_CKE_A1
SA_CKE_2	AU18	M_CKE_A1
SA_CKE_3	AV18	M_CKE_A1

SA_ODT_0	AV31	M_ODT_A0
SA_ODT_1	AU30	M_ODT_A1
SA_ODT_2	AW33	M_ODT_A1
SA_ODT_3	AW33	M_ODT_A1

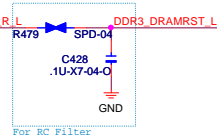
SA_CLK_0	AY25	M_CLK_A_P0
SA_CLK#_0	AW25	M_CLK_A_P0
SA_CLK#_1	AU24	M_CLK_A_P1
SA_CLK#_2	AU25	M_CLK_A_N1
SA_CLK#_3	AW27	M_CLK_A_N1
SA_CLK#_4	AY27	M_CLK_A_P0
SA_CLK#_5	AV26	M_CLK_A_P0
SA_CLK#_6	AW26	M_CLK_A_P0

SM_DRAMRST# ← AW18DDR3_DRAMRST_R L

SA_DQS_8	AV13	SA_DQS#_8
SA_DQS#_8	AV12	SA_DQS#_8
SA_ECC_CB_0	AU12	SA_ECC_CB_0
SA_ECC_CB_1	AU14	SA_ECC_CB_1
SA_ECC_CB_2	AW13	SA_ECC_CB_2
SA_ECC_CB_3	AY13	SA_ECC_CB_3
SA_ECC_CB_4	AU13	SA_ECC_CB_4
SA_ECC_CB_5	AU11	SA_ECC_CB_5
SA_ECC_CB_6	AY12	SA_ECC_CB_6
SA_ECC_CB_7	AW12	SA_ECC_CB_7

DDR_0

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Desktop doesn't support ecc

Pay Attention to This Part!

CPUID

BALLMAP_REV=1.7

M_DATA_B0	AG7	SB_DQ_0
M_DATA_B1	AG8	SB_DQ_1
M_DATA_B2	AJ9	SB_DQ_2
M_DATA_B3	AJ8	SB_DQ_3
M_DATA_B4	AG5	SB_DQ_4
M_DATA_B5	AG6	SB_DQ_5
M_DATA_B6	AJ6	SB_DQ_6
M_DATA_B7	AJ7	SB_DQ_7
M_DATA_B13	AL7	SB_DQ_8
M_DATA_B9	AM7	SB_DQ_9
M_DATA_B11	AM10	SB_DQ_10
M_DATA_B15	AL10	SB_DQ_11
M_DATA_B12	AL15	SB_DQ_12
M_DATA_B8	AM6	SB_DQ_13
M_DATA_B14	AL9	SB_DQ_14
M_DATA_B10	AM9	SB_DQ_15
M_DATA_B16	AR7	SB_DQ_16
M_DATA_B17	AR7	SB_DQ_17
M_DATA_B18	AP10	SB_DQ_18
M_DATA_B19	AR10	SB_DQ_19
M_DATA_B20	AP6	SB_DQ_20
M_DATA_B21	AR6	SB_DQ_21
M_DATA_B22	AP9	SB_DQ_22
M_DATA_B23	AR9	SB_DQ_23
M_DATA_B24	AM12	SB_DQ_24
M_DATA_B25	AM13	SB_DQ_25
M_DATA_B26	AR13	SB_DQ_26
M_DATA_B27	AP13	SB_DQ_27
M_DATA_B28	AL12	SB_DQ_28
M_DATA_B29	AL13	SB_DQ_29
M_DATA_B30	AR12	SB_DQ_30
M_DATA_B31	AP12	SB_DQ_31
M_DATA_B32	AR28	SB_DQ_32
M_DATA_B33	AR29	SB_DQ_33
M_DATA_B34	AL28	SB_DQ_34
M_DATA_B35	AL29	SB_DQ_35
M_DATA_B36	AP28	SB_DQ_36
M_DATA_B37	AP29	SB_DQ_37
M_DATA_B38	AM28	SB_DQ_38
M_DATA_B39	AM29	SB_DQ_39
M_DATA_B40	AP32	SB_DQ_40
M_DATA_B41	AP31	SB_DQ_41
M_DATA_B42	AP35	SB_DQ_42
M_DATA_B43	AP34	SB_DQ_43
M_DATA_B44	AR32	SB_DQ_44
M_DATA_B45	AR31	SB_DQ_45
M_DATA_B46	AR35	SB_DQ_46
M_DATA_B47	AR34	SB_DQ_47
M_DATA_B48	AM32	SB_DQ_48
M_DATA_B52	AM31	SB_DQ_49
M_DATA_B55	AL35	SB_DQ_50
M_DATA_B51	AL32	SB_DQ_51
M_DATA_B54	AM34	SB_DQ_52
M_DATA_B49	AL31	SB_DQ_53
M_DATA_B53	AM35	SB_DQ_54
M_DATA_B50	AL34	SB_DQ_55
M_DATA_B56	AE35	SB_DQ_56
M_DATA_B57	AE34	SB_DQ_57
M_DATA_B58	AE34	SB_DQ_58
M_DATA_B59	AE35	SB_DQ_59
M_DATA_B60	AJ34	SB_DQ_60
M_DATA_B61	AF33	SB_DQ_61
M_DATA_B62	AF33	SB_DQ_62
M_DATA_B63	AF35	SB_DQ_63

SB_WE#_0	AR25	M_WE_B_L
SB_CAS#_0	AK25	M_CAS_B_L
SB_RAS#_0	AP24	M_RAS_B_L

SB_BS_0	AP23	M_BS_B0
SB_BS_1	AM24	M_BS_B1
SB_BS_2	AW17	M_BS_B2

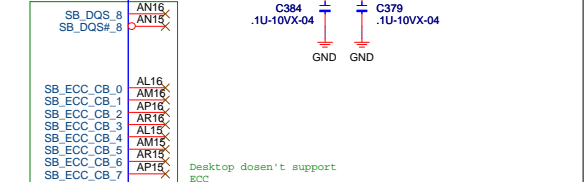
SB_CS#_0	AN25	M_CS_B_L0
SB_CS#_1	AN26	M_CS_B_L1
SB_CS#_2	AT25	M_CS_B_L1
SB_CS#_3	AT26	M_CS_B_L1

SB_CKE_0	AU16	M_CKE_B0
SB_CKE_1	AY15	M_CKE_B1
SB_CKE_2	AW15	M_CKE_B1
SB_CKE_3	AV15	M_CKE_B1

SB_ODT_0	AL26	M_ODT_B0
SB_ODT_1	AP26	M_ODT_B1
SB_ODT_2	AM26	M_ODT_B1
SB_ODT_3	AK26	M_ODT_B1

SB_CLK_0	AL21	M_CLK_B_P0
SB_CLK#_0	AL22	M_CLK_B_N0
SB_CLK#_1	AL20	M_CLK_B_P1
SB_CLK#_2	AK20	M_CLK_B_N1
SB_CLK#_3	AL23	M_CLK_B_N1
SB_CLK#_4	AM22	M_CLK_B_N1
SB_CLK#_5	AP21	M_CLK_B_N1
SB_CLK#_6	AN21	M_CLK_B_N1

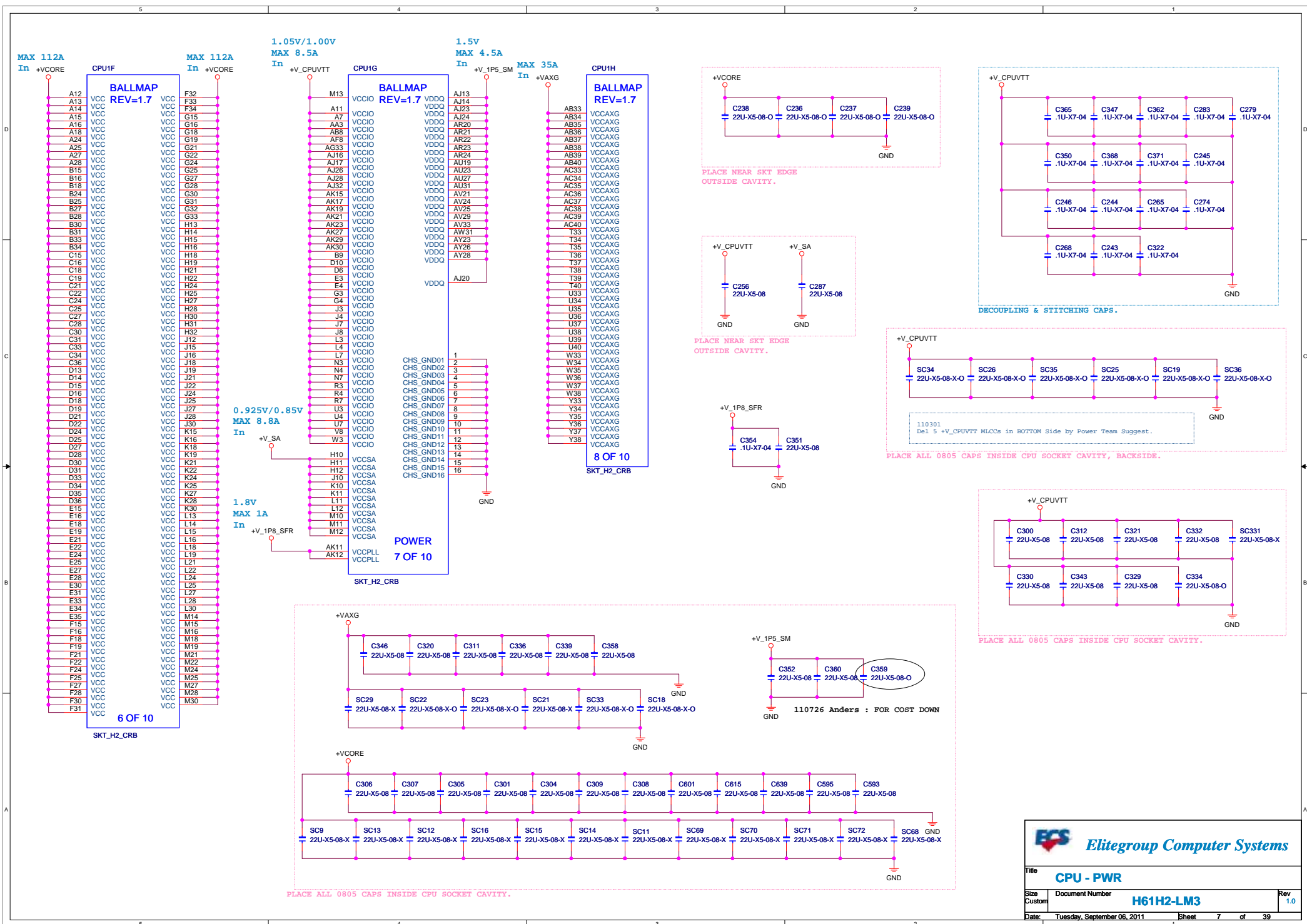
SB_DIMM_DQVREF ← AH1 DIMM_DQ_CPU_VREF_B
SA_DIMM_DQVREF ← AH4 DIMM_DQ_CPU_VREF_A

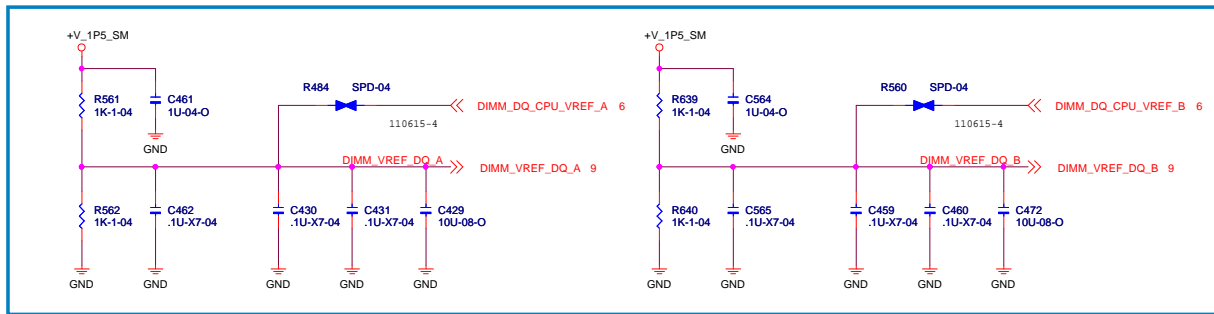


DDR_1

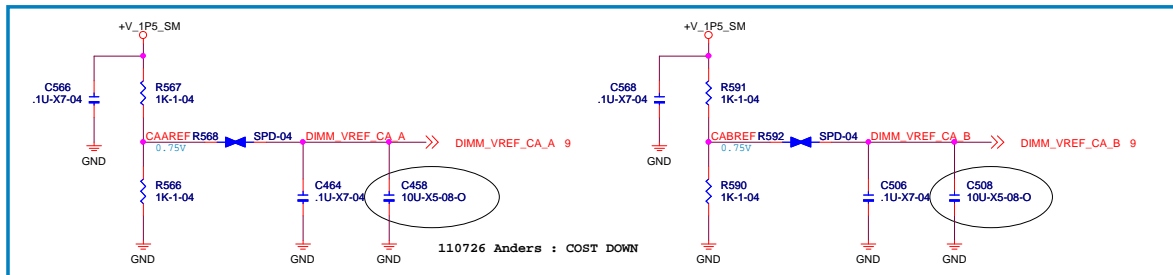
4 OF 10

SKT_H2_CRB

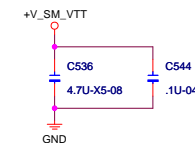
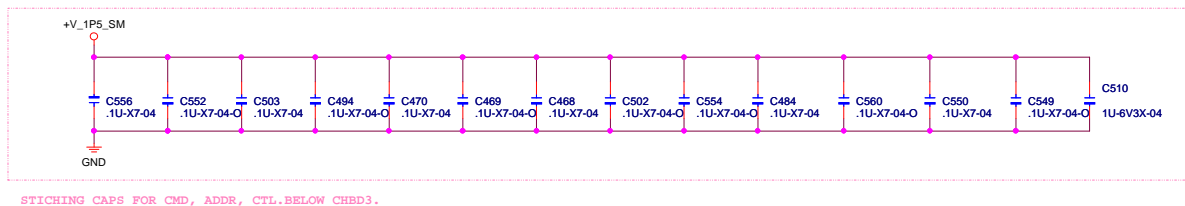
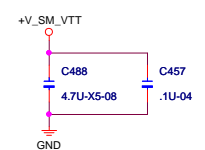
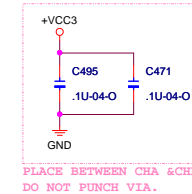
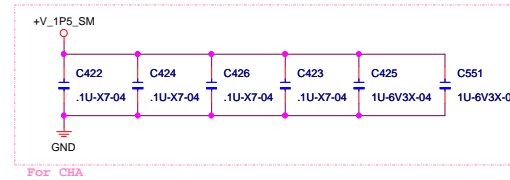
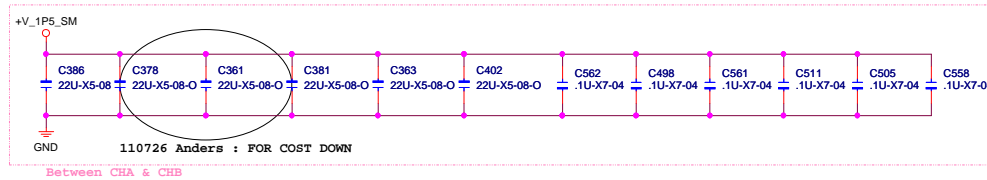


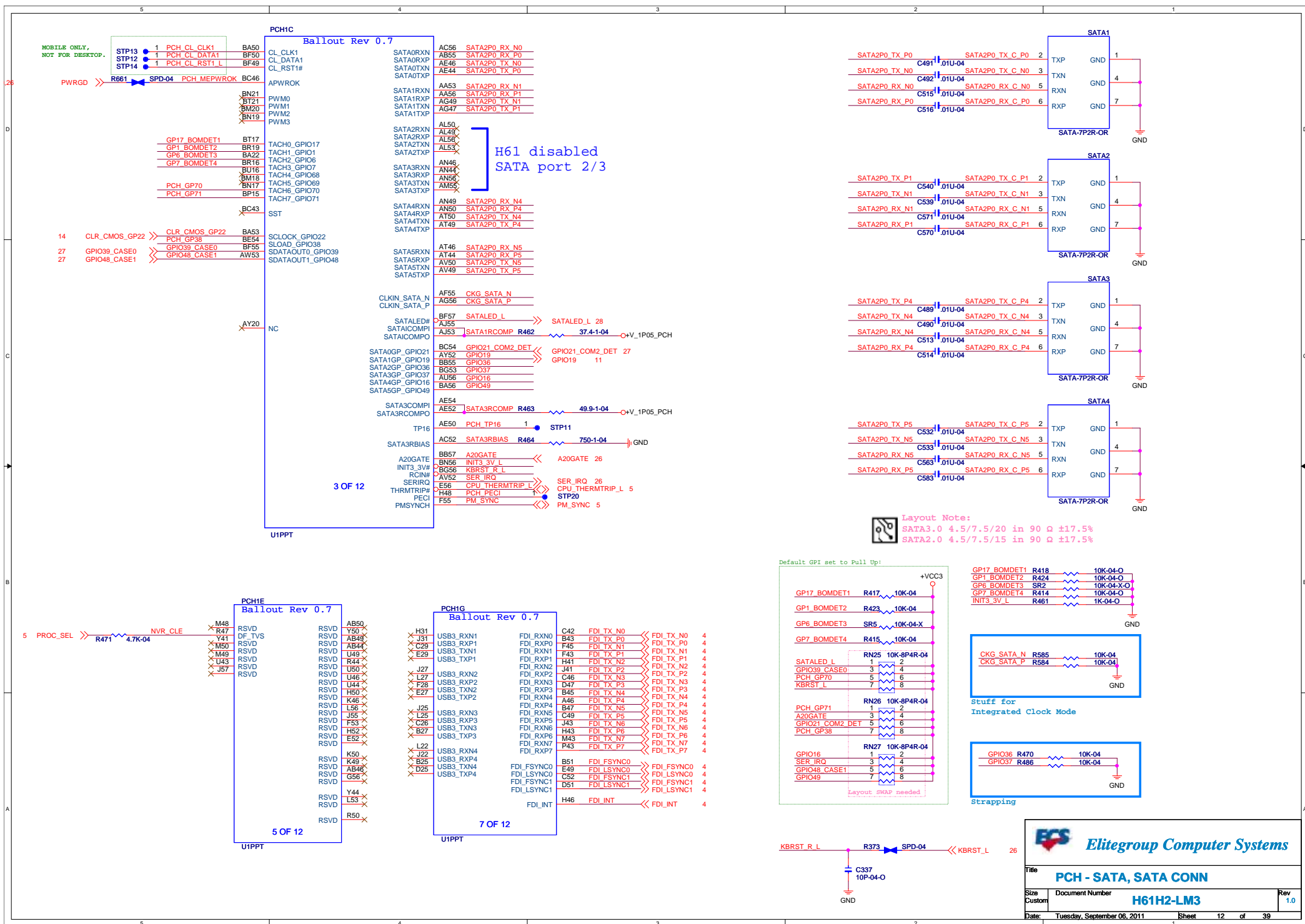


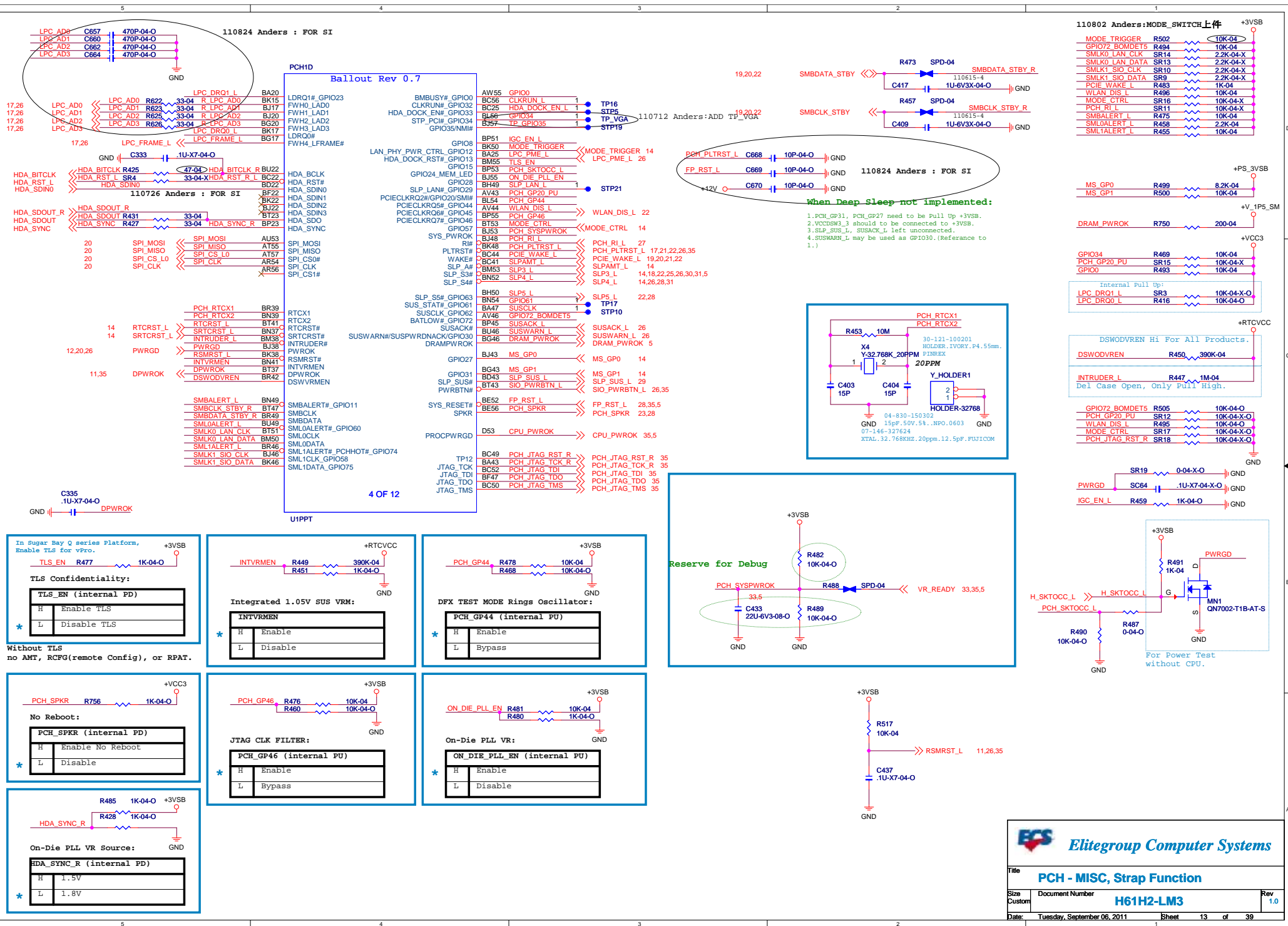
DIMM_VREF_DQ Control Circuit

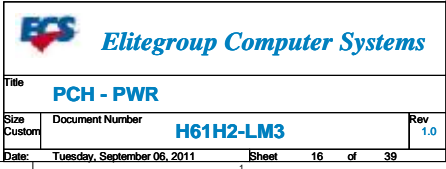


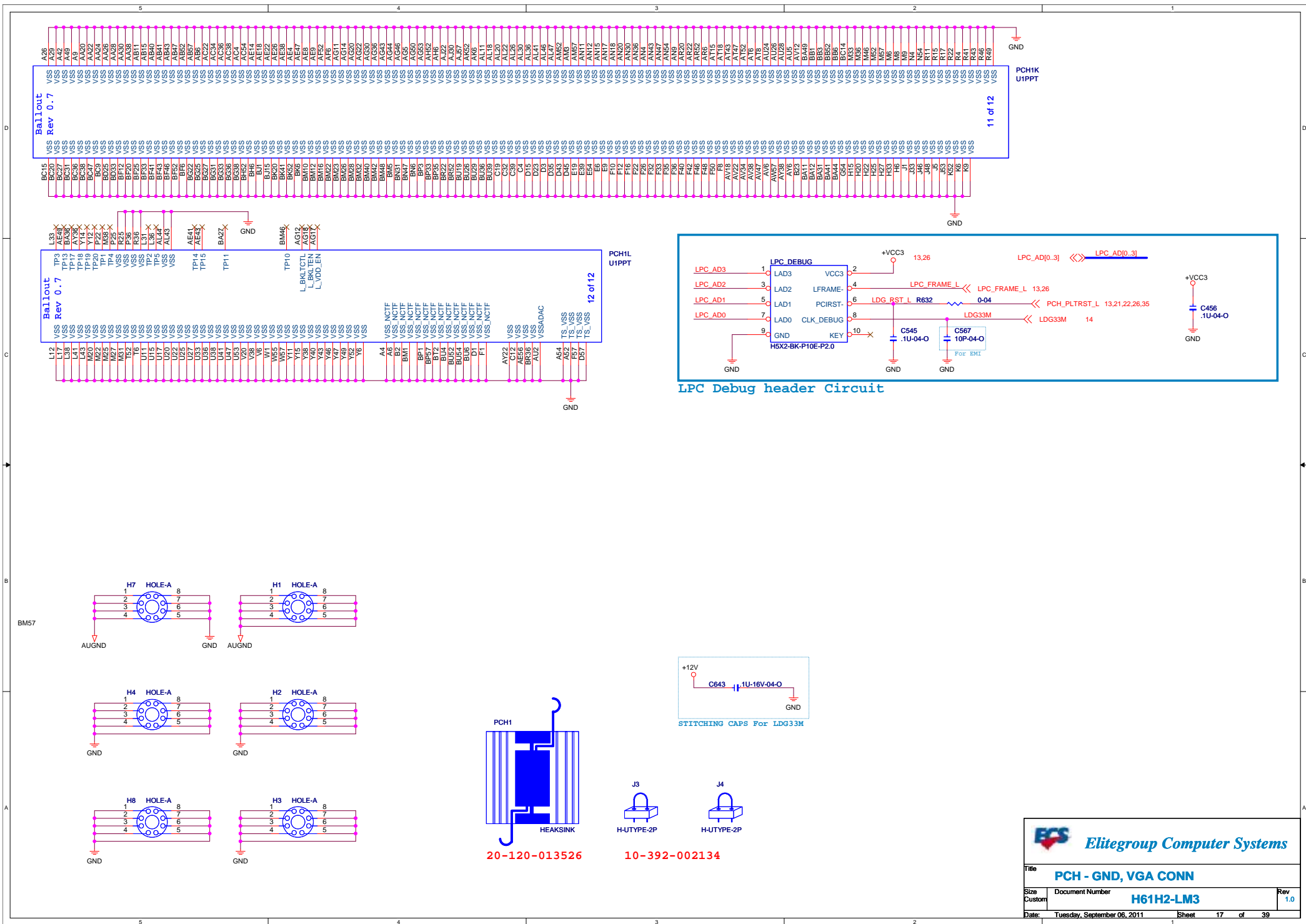
DIMM_VREF_CA Circuit



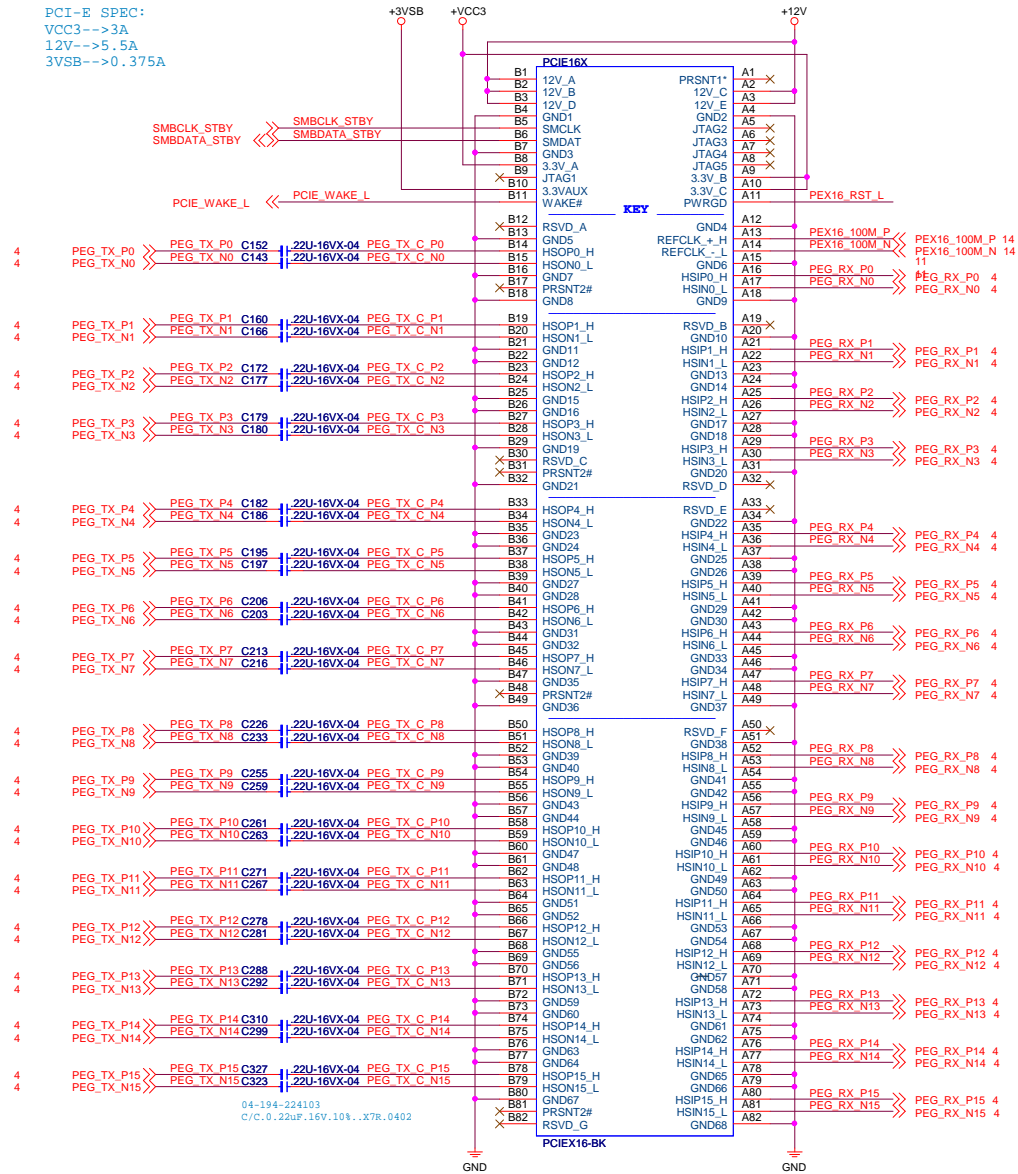




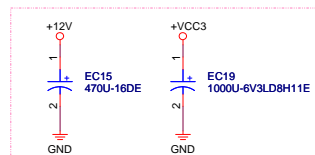




PCI-E SPEC:
VCC3-->3A
12V-->5.5A
3VSB-->0.375A

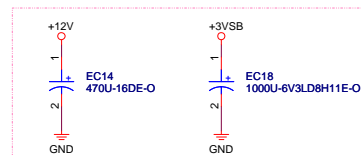


04-711-102073
E/C.1000uF.16V.20%...105C.RT D10*17mm....

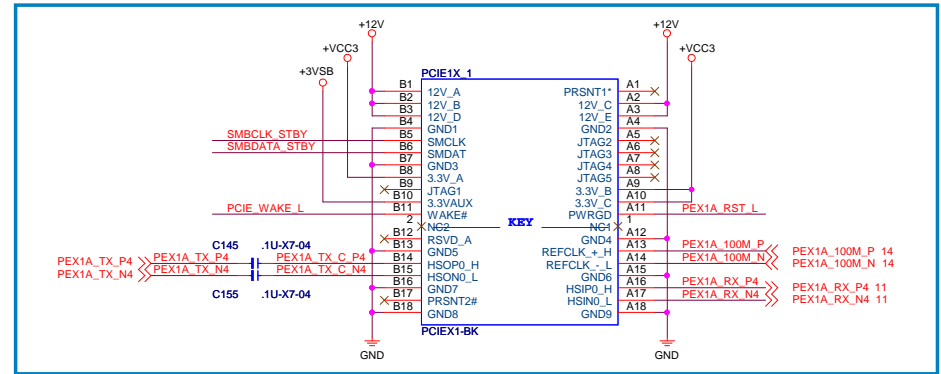


Between PEX16 & PEX1A

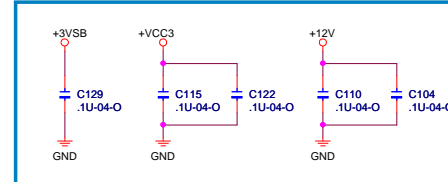
04-711-102073
E/C.1000uF.16V.20%...105C.RT D10*17mm....



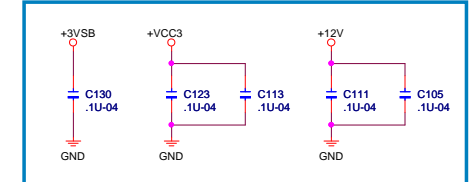
Between PEX1A & PEX1B



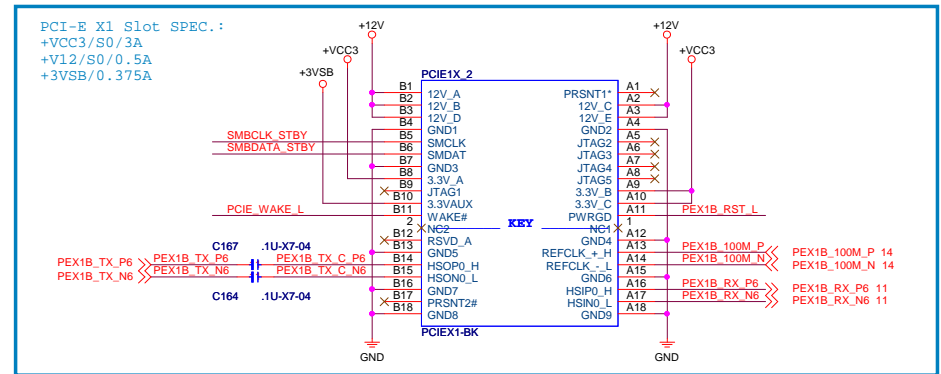
PCI-E X1 A



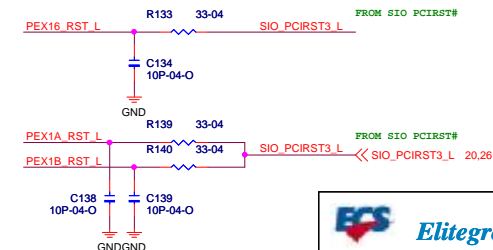
PCI-E X1 A Decoupling Cap.



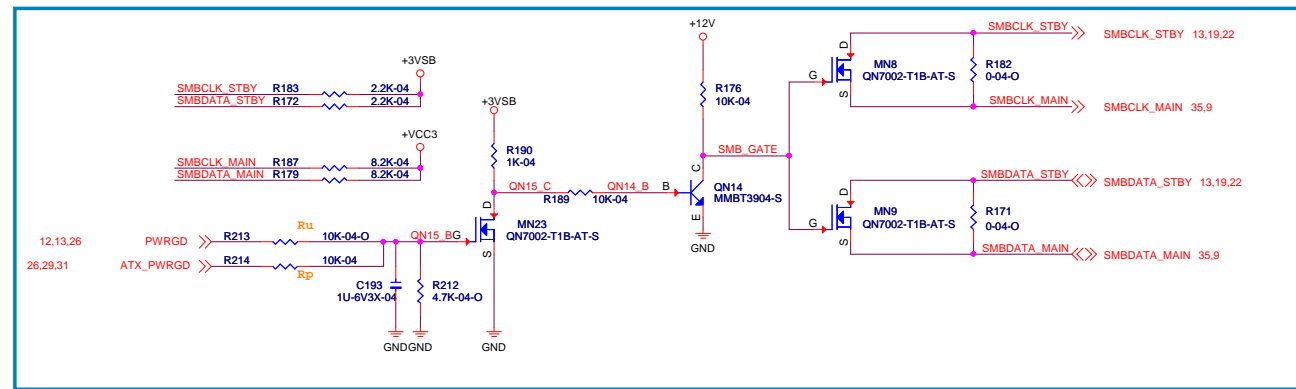
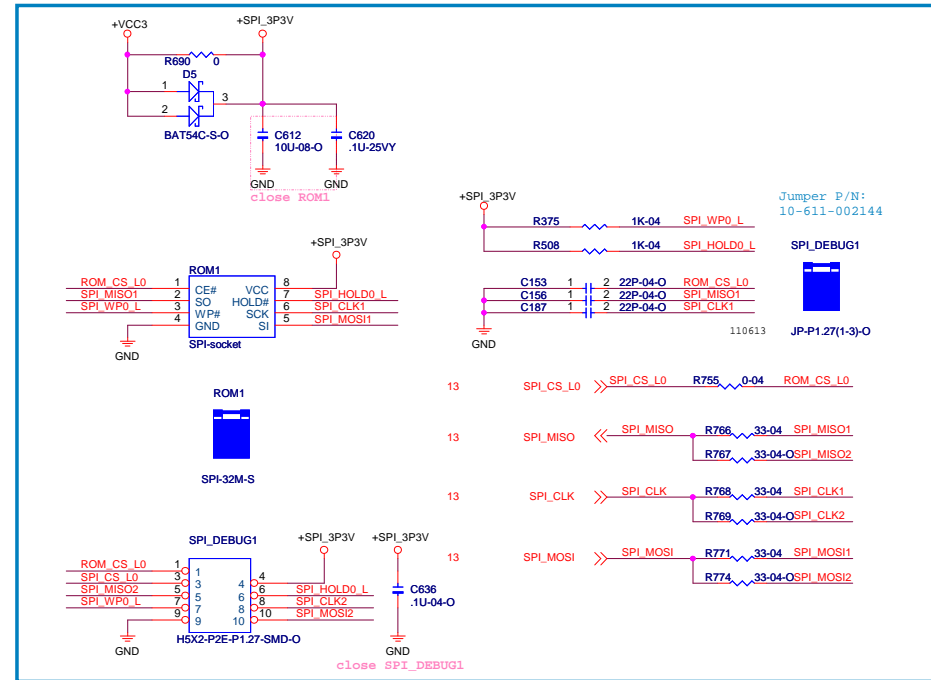
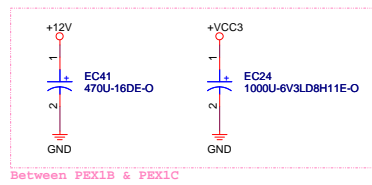
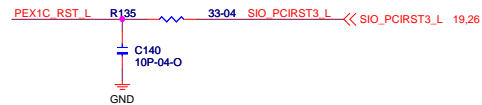
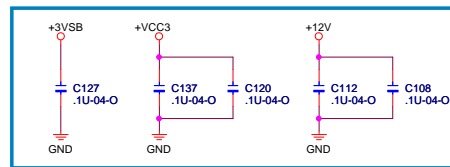
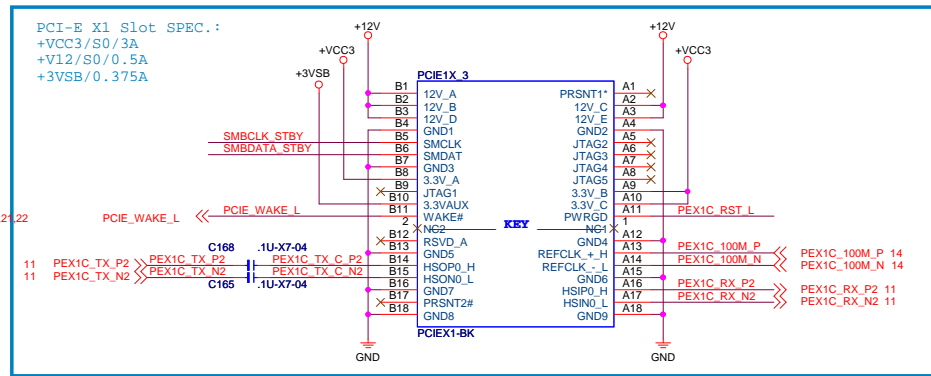
PCI-E X1 B Decoupling Cap.

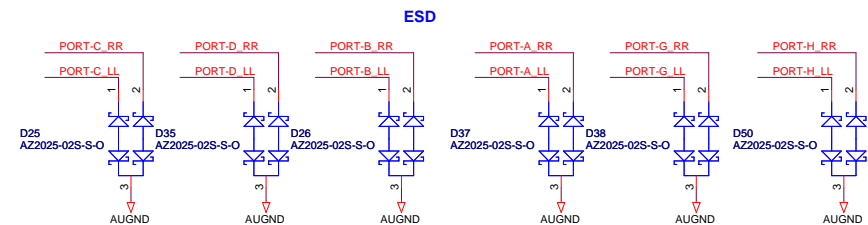
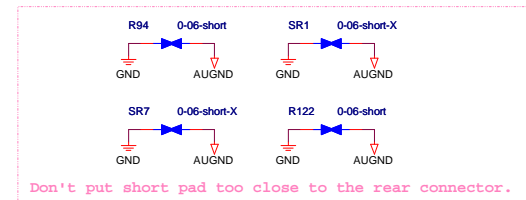
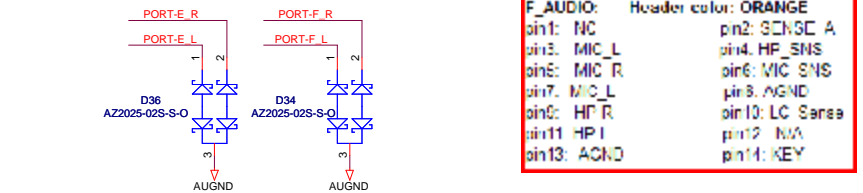
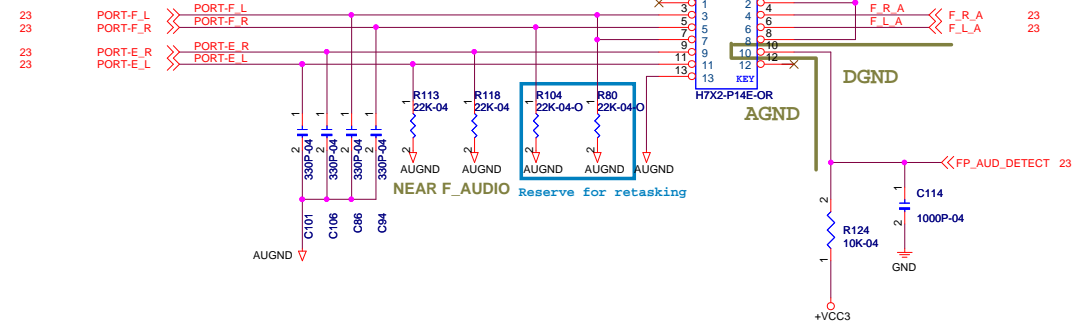


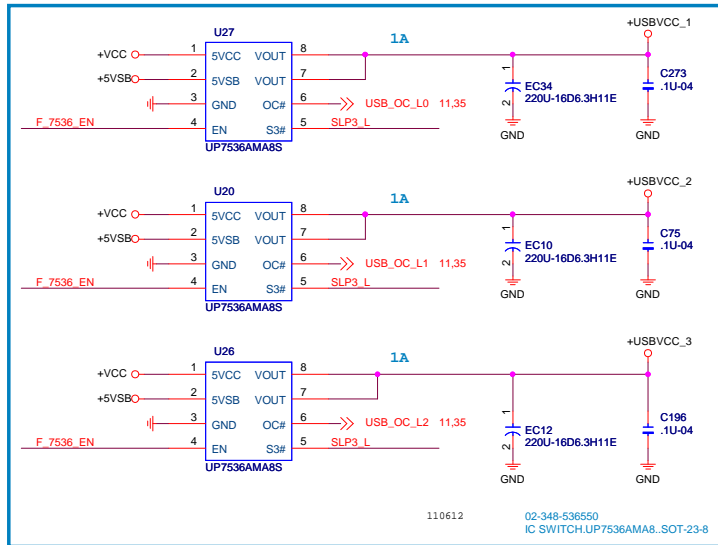
PCI-E X1 B



Title Slot - PCI-EX16/PCI-EX1			
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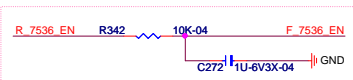
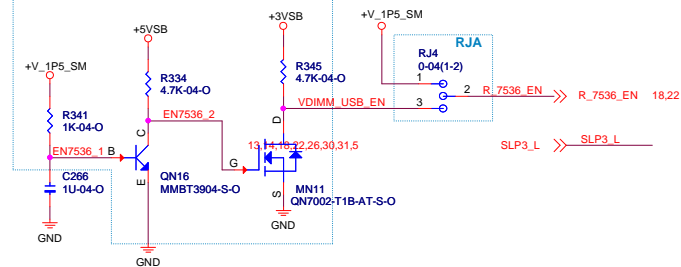




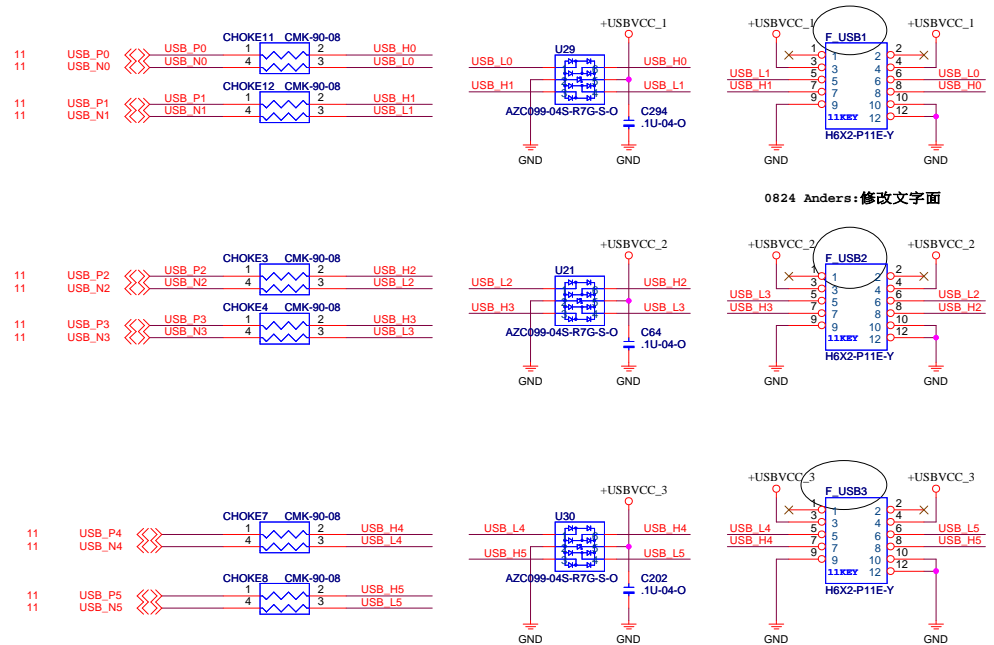
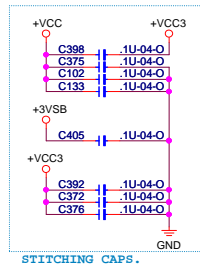


USB2.0 POWER CIRCUIT

Level shift



uP7536 Enable use	Level shift	RJA	RJB	S4/S5 USB_5V_DUAL	Customer
VDIMM	N A	0ohm (1-2)	N A	0 Volt	Lenovo S4/S5 w/o USB_5V_DUAL
VDIMM level shift (3.3V)	Stuff	0ohm (2-3)	N A	0 Volt	



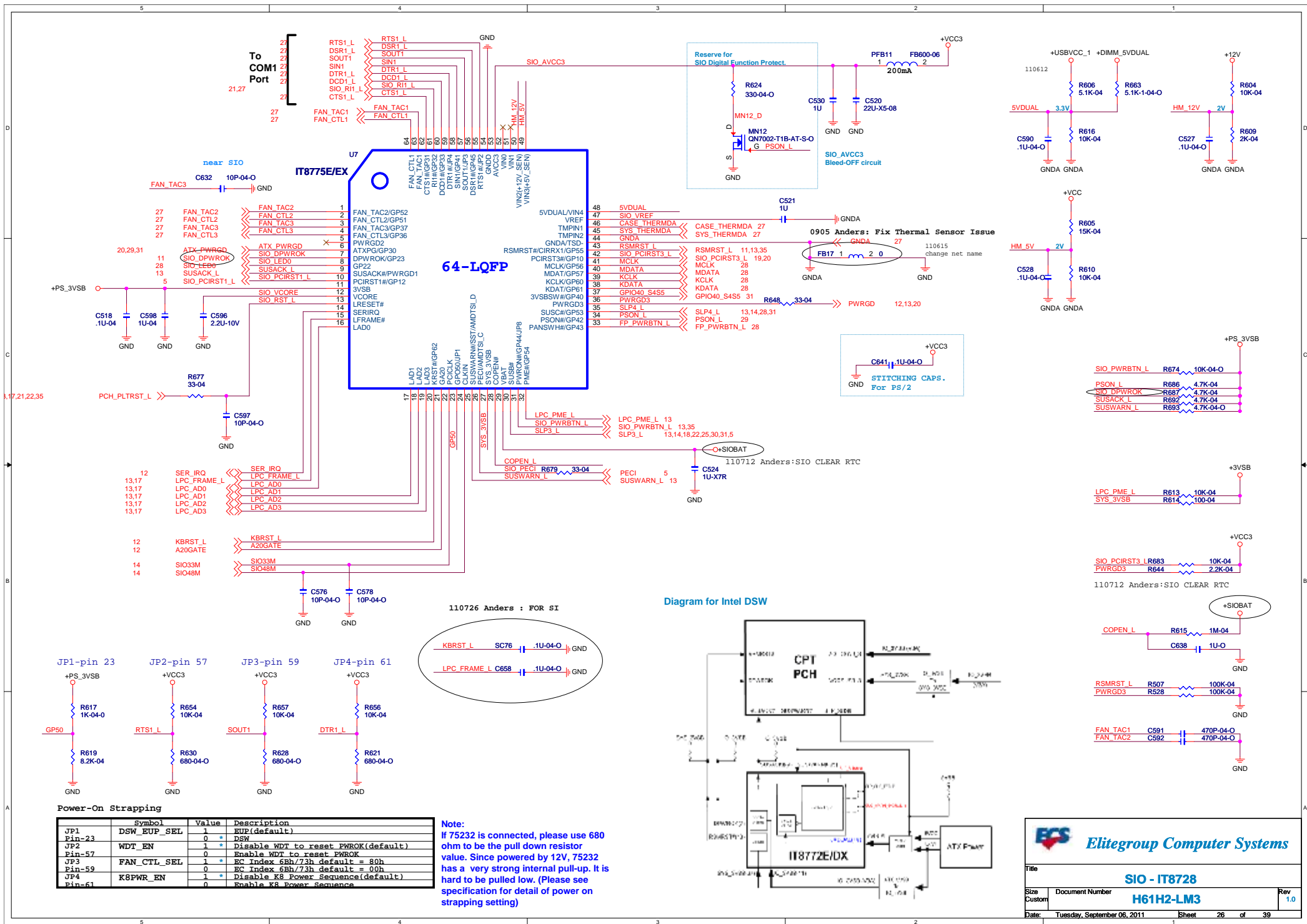
FRONT SIDE 4 PORTS USB2.0 Header

03-012-702517 Value:TVS,AZ2025-01H..5V.SOD-523 Footprint: SOD_523

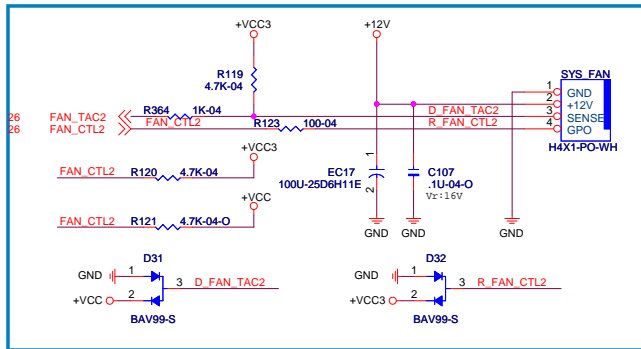


USB Header Power ESD protection diode.

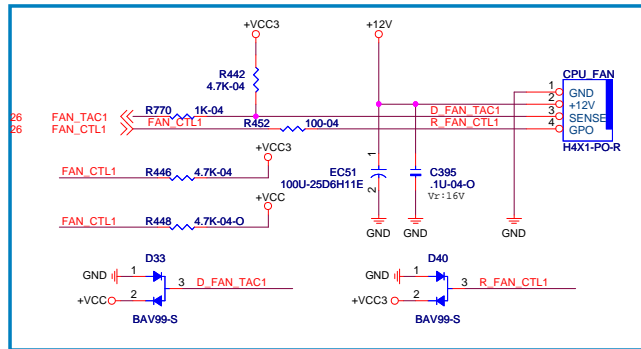
Title	
USB2.0 - header	
Size Custom	Document Number
	H61H2-LM3
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	Rev 1.0



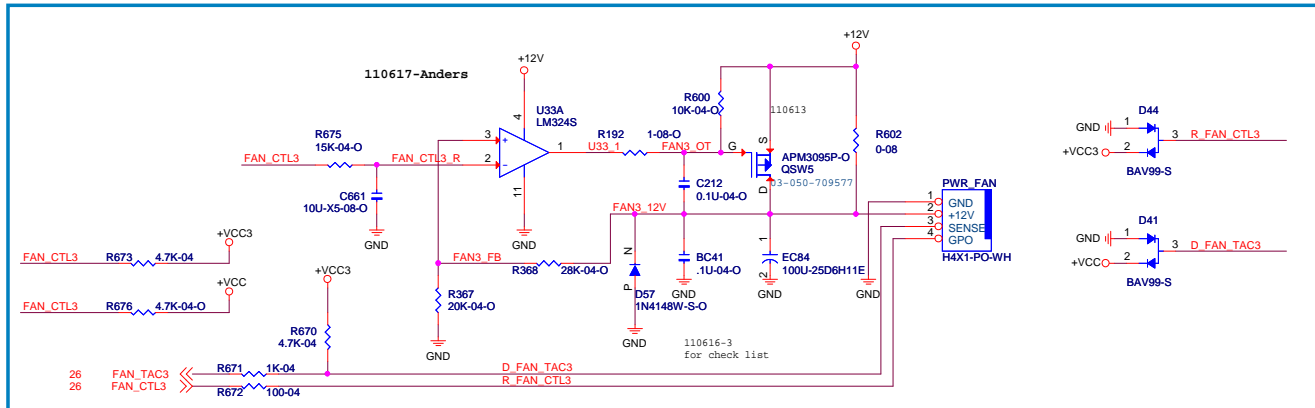
Note:
If 75232 is connected, please use 680 ohm to be the pull down resistor value. Since powered by 12V, 75232 has a very strong internal pull-up. It is hard to be pulled low. (Please see specification for detail of power on strapping setting)



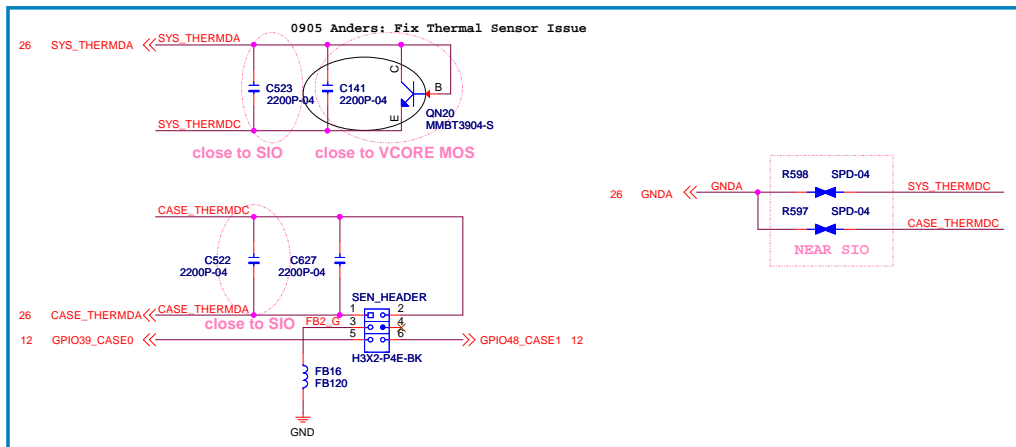
SYS FAN 4-PIN Circuit



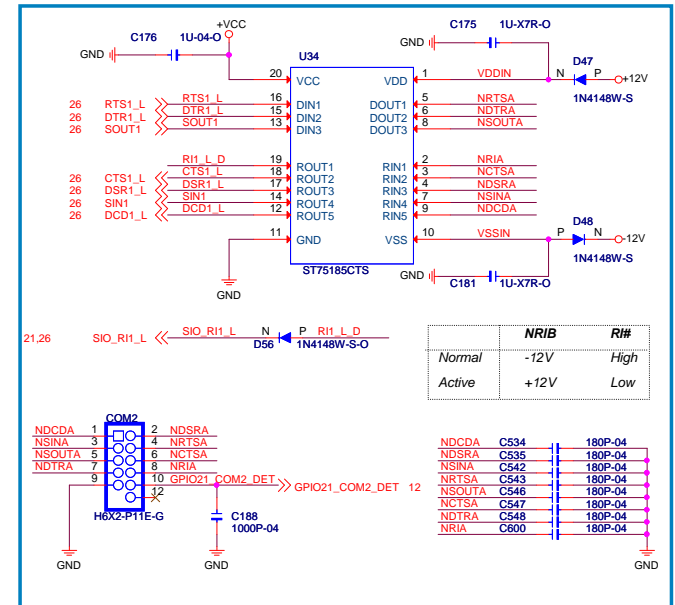
CPU FAN 4-PIN Circuit



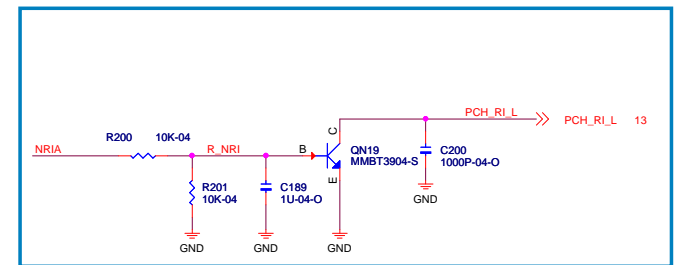
PWR FAN 3,4 pin co-layout circuit



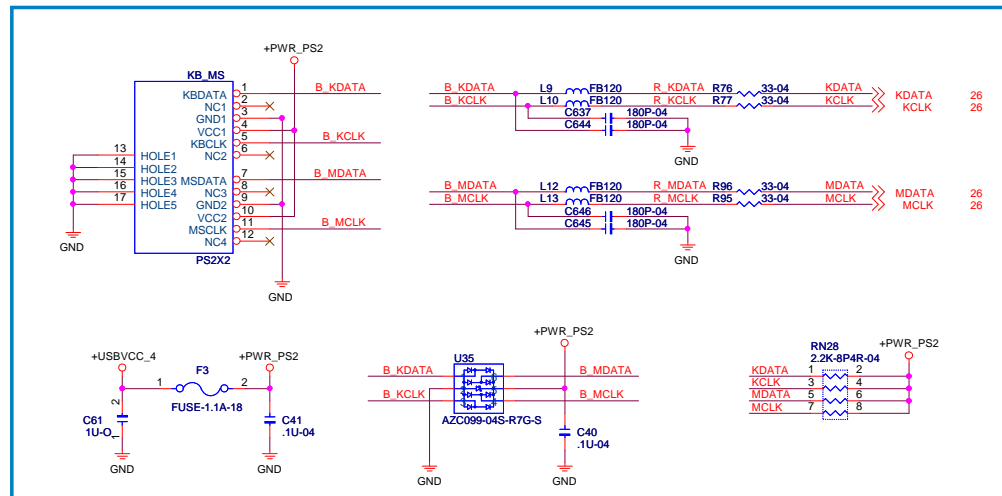
Thermal Sense



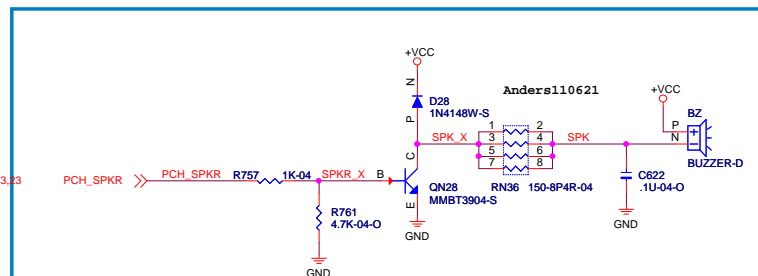
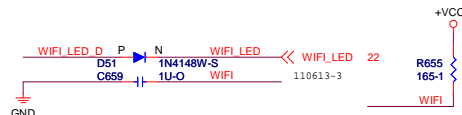
COM Header Circuit



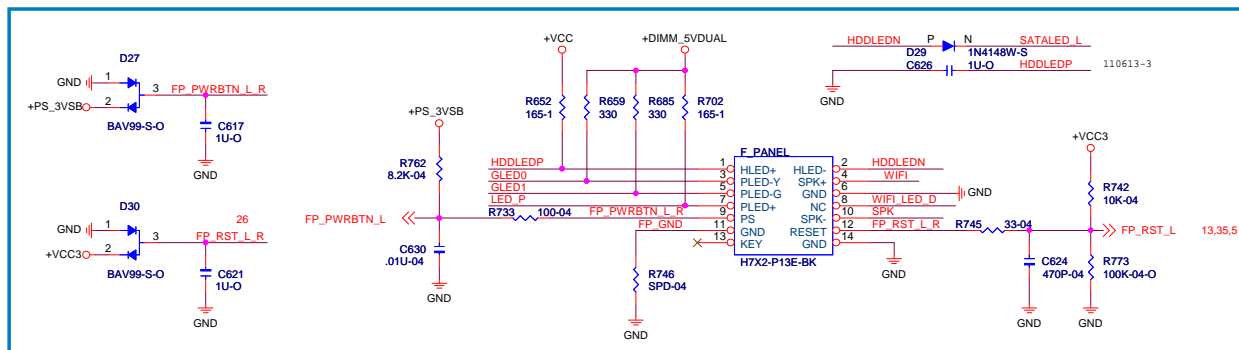
COM2 RI# Wake Up Circuit



PS/2 Connector

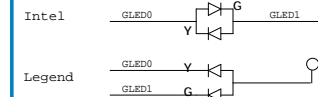


Buzzer Circuit

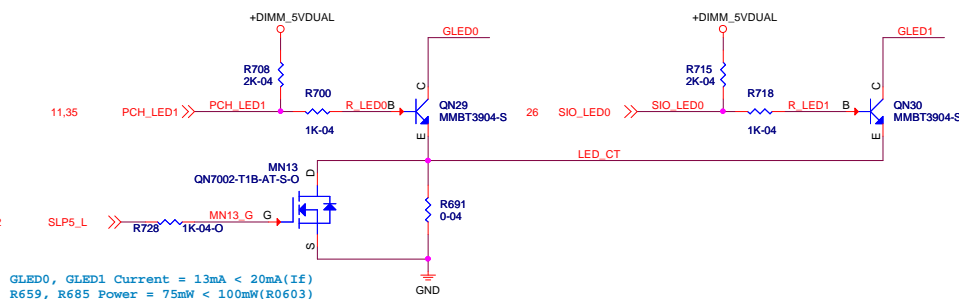


Front Panel Circuit

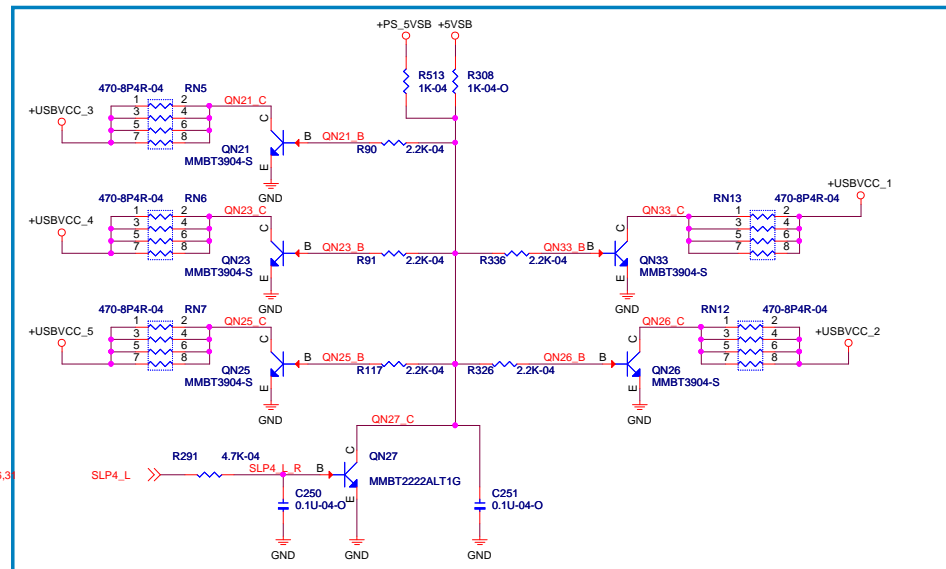
3-Pin Dual color LED	
S0	Steady Green
S1	Green-blinking
S3	Steady Yellow
S4,S5	Off
2-Pin single color LED	
S0	Steady Green
S1,S3	LED-blinking
S4,S5	Off



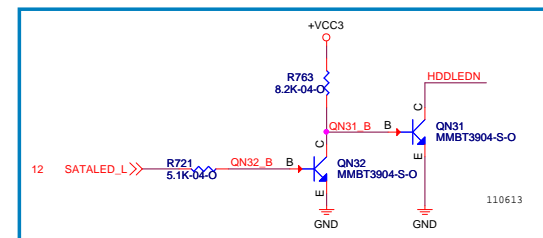
Front LED



GLEDD0, GLEDD1 Current = 13mA < 20mA(If)
R659, R685 Power = 75mW < 100mW(R0603)



USB Discharge Circuit



SATA LED Blink Once in Power On Issue

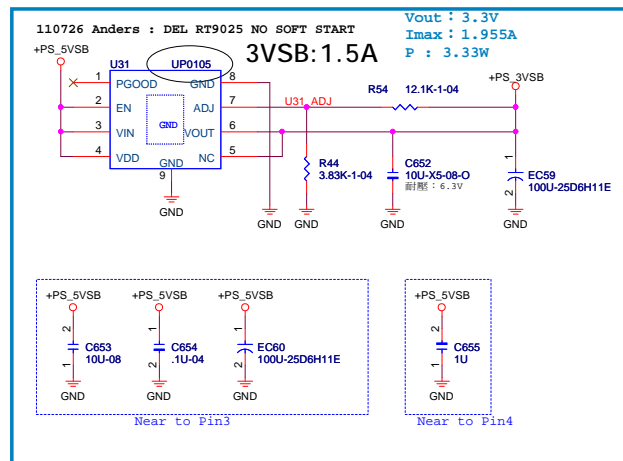
Elitegroup Computer Systems

F_PANEL, BUZ, PS2, USB Discharge

Document Number **H61H2-LM3**

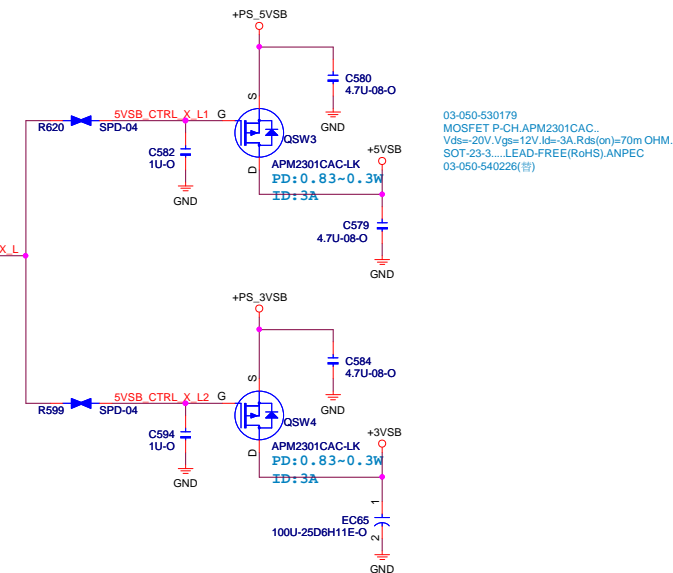
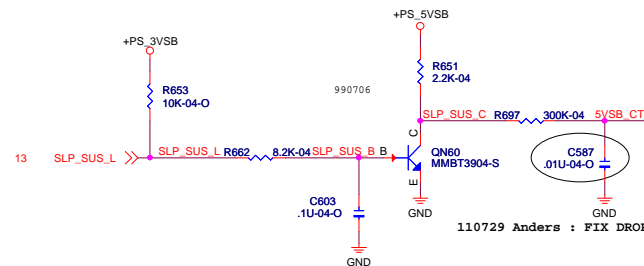
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3VSB (S0):

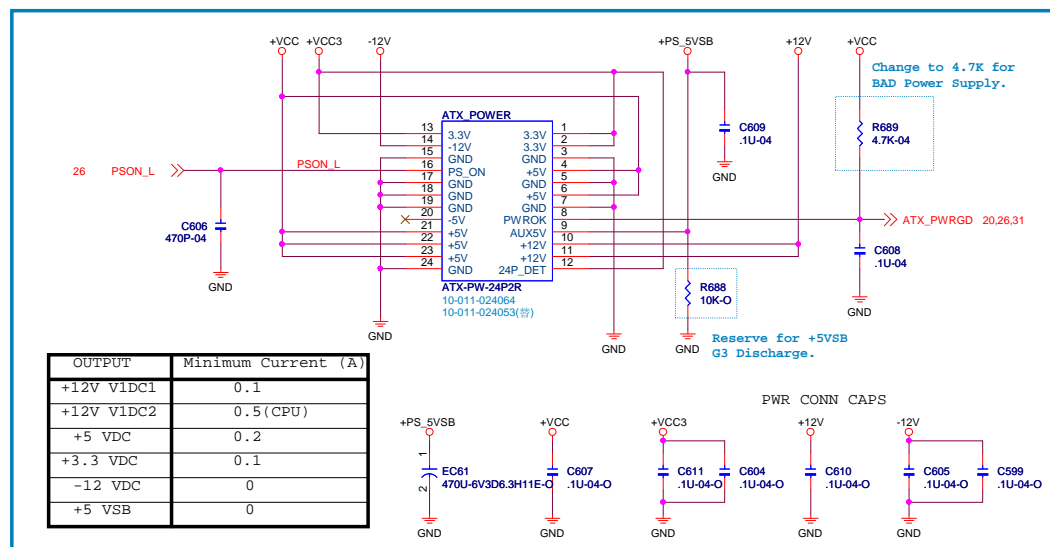
Power Name	Current
PCH	105mA
LAN RTL8111E-VL	165mA
SIO IT8772EX	6mA
EPW Non-AMT	0mA
SPI Non-AMT	0mA
PCI-E 4 Slots	0.375 X 4 = 1.5A
MINI PCI-E 1 Slots	1.1A
Total Current	0.28 + 2.6 = 2.88A



BuP Lot6 2013 0.5W:

PWR STATE	+5VSB Source
S0	+PS 5VSB
S3	+PS 5VSB
S4	OFF
S5	OFF

Layout Note:
Close to ATX 24P2R Connector.



OUTPUT	Minimum Current (A)
+12V V1DC1	0.1
+12V V1DC2	0.5 (CPU)
+5 VDC	0.2
+3.3 VDC	0.1
-12 VDC	0
+5 VSB	0

ATX Power 24PIN

Default Stuffed:

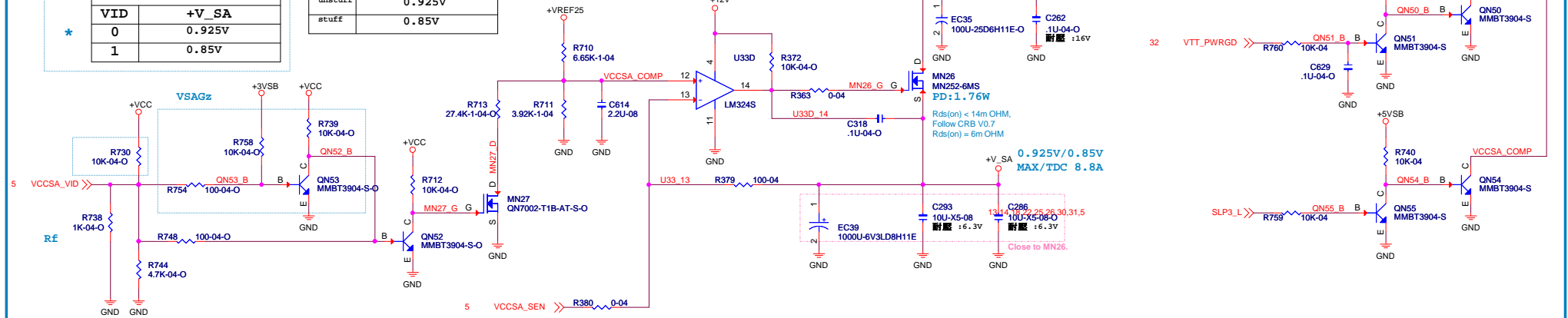
Stuff VSAGz

VCCSA voltage selection

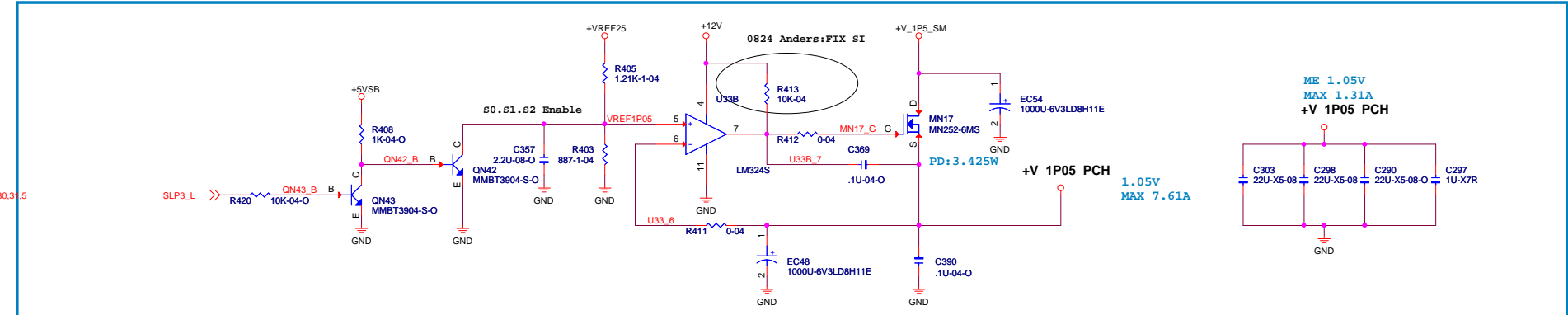
VID	+V_SA
0	0.925V
1	0.85V

VCCSA voltage selection

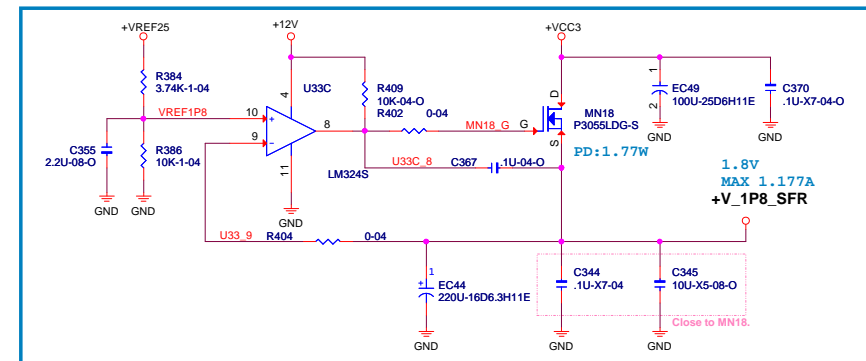
Rf	+V_SA
unstuff	0.925V
stuff	0.85V



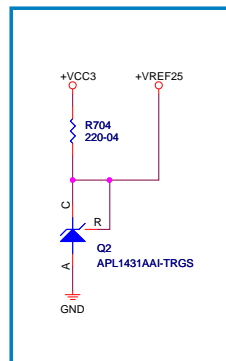
+V_SA



+V_1P05_PCH

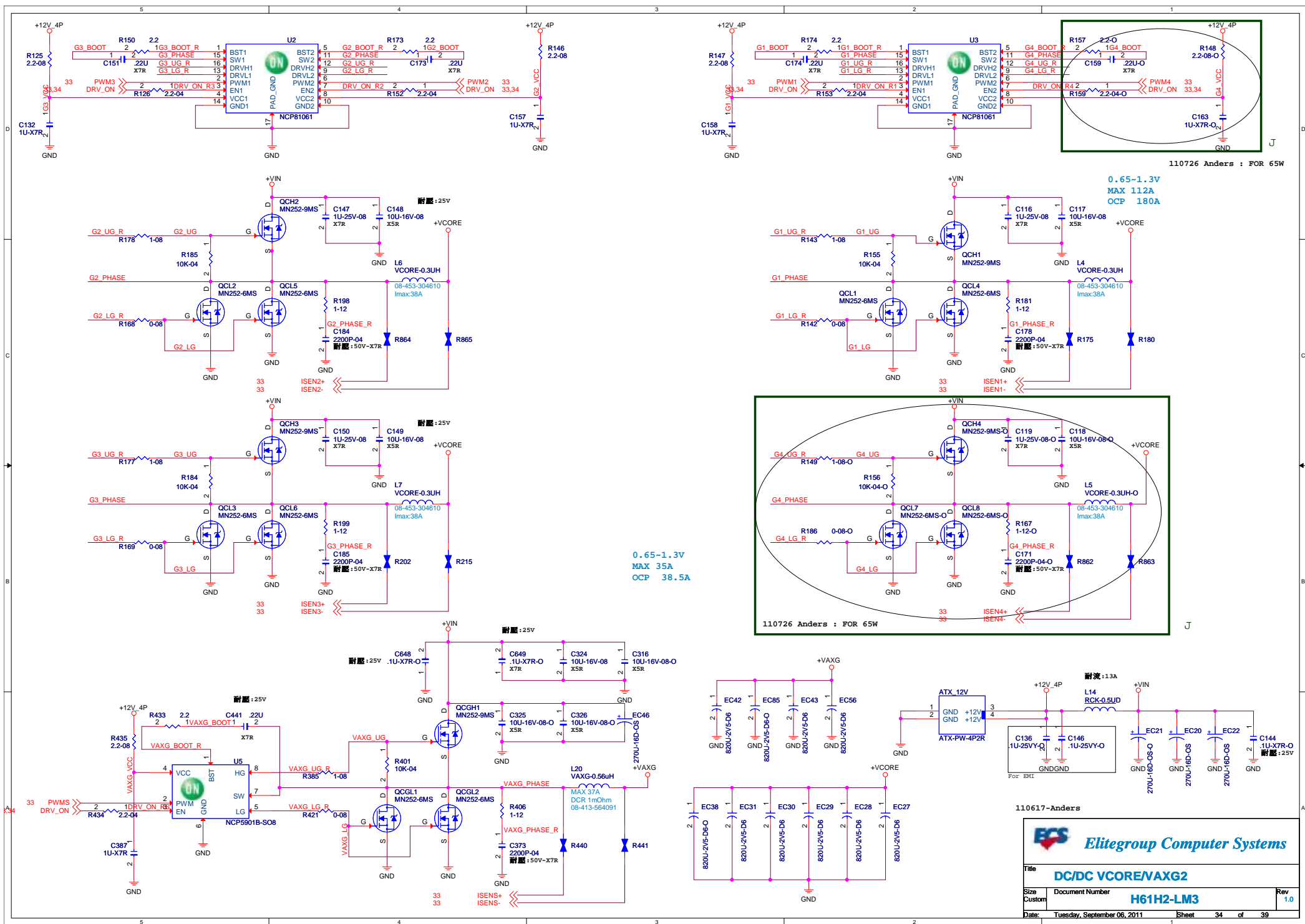


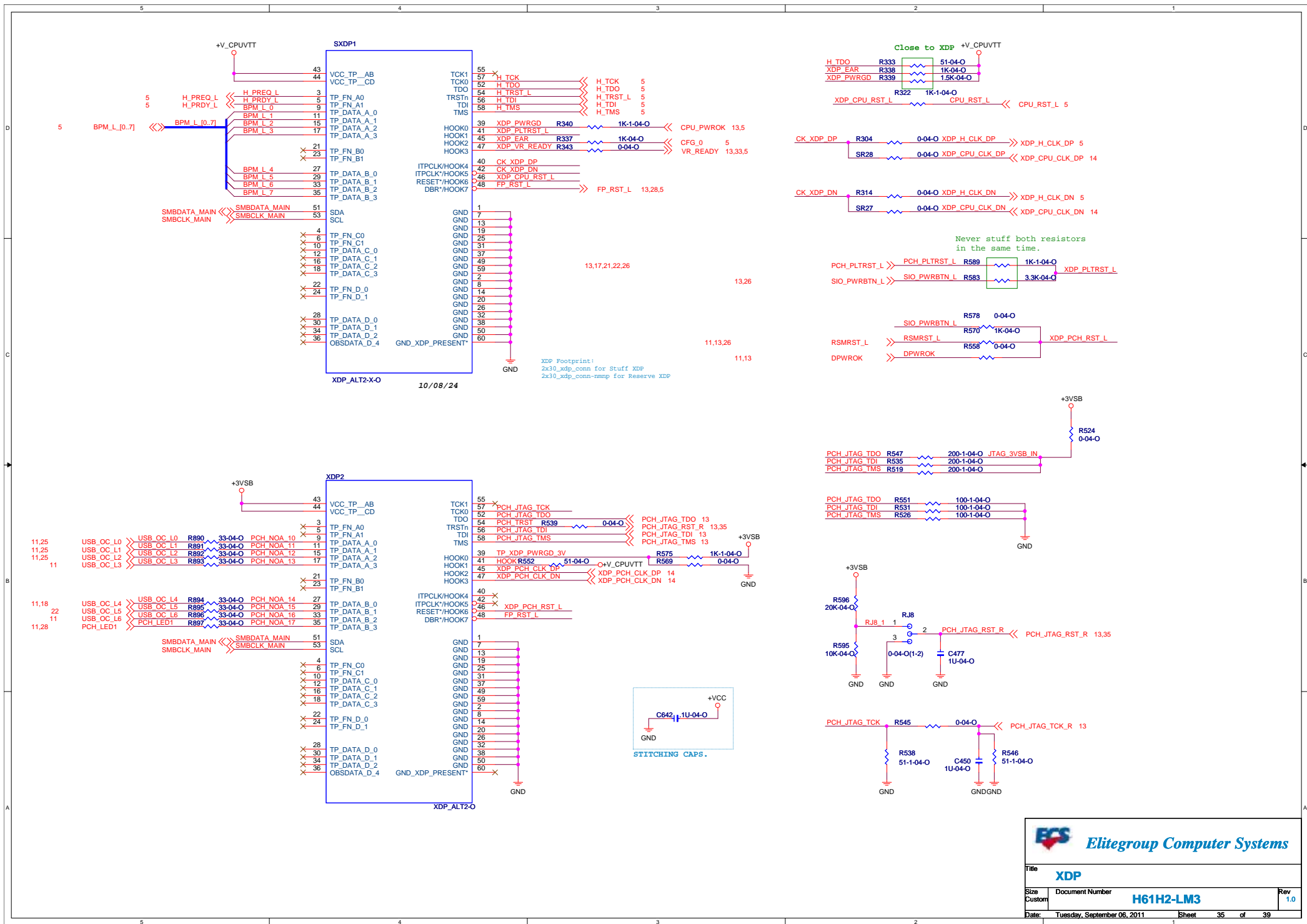
+V1P8_SFR(1.6A max)



VREF25

02-348-431705
Value:IC REG.APL1431AAI-TRL_SOT-23_2.5V
Footprint: SOT23_RAC_Z_2





PCH Strap Pin

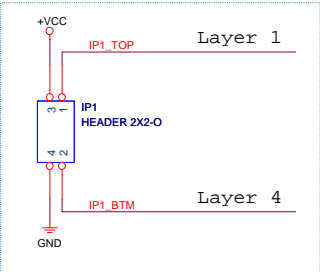
Pin Name	Usage	Default Status
SPKR	No Reboot	20K internal pull-down , No Reboot Mode with TCO Disabled:
INIT3_3V#	Reserved	20K internal pull-up , intend for Firmware Hub.
GNT[3]#/GPIO[55]	Disable Top-Block Swap	20K internal pull-up , "topblock swap" mode Disable
INTVRMEN	Enable Integrated 1.05V VRM	Need External Pull-up , Integrated 1.05V VRM Enable
GNT1# /GPIO51	Boot BIOS Strap bit [1] BBS[1]	20K internal pull-up , The default flash selection is the SPI flash.All
SATA1GP / GPIO19	Boot BIOS Strap bit[0] BBS[0]	20K internal pull-up , The default flash selection is the SPI flash.All
HDA_SDO	Flash Descriptor Security Override/ ME	Internal pull-down. The security measures defined in the Flash Descriptor will be in effect(default)
DF_TV5	Enable DMI termination voltage	This signal has a weak internal pull-down.
GPIO28	Eable On-Die PLL Voltage Regulator	The On-Die PLL voltage regulator is enabled
HDA_SYNC	On-Die PLL Voltage Regulator Voltage Select 1.8V	20K internal pull-down.On Die PLL VR is supplied by 1.5 V when sampled high, 1.8 V when sampled low.
GPIO15	Disable TLS Confidentiality	Intel Management Engine Crypto Transport Layer Security (TLS) cipher suite with no confidentiality.

SIO Strap Pin

Power-On Strapping

	Symbol	Value	Description
JP1	DSW_EUP_SEL	1	EUP(default)
Pin-23		0 *	DSW
JP2	WDT_EN	1 *	Disable WDT to reset PWROK(default)
Pin-57		0	Enable WDT to reset PWROK
JP3	FAN_CTL_SEL	1 *	EC Index 6Bh/73h default = 80h
Pin-59		0	EC Index 6Bh/73h default = 00h
JP4	K8PWR_EN	1 *	Disable K8 Power Sequence(default)
Pin-61		0	Enable K8 Power Sequence

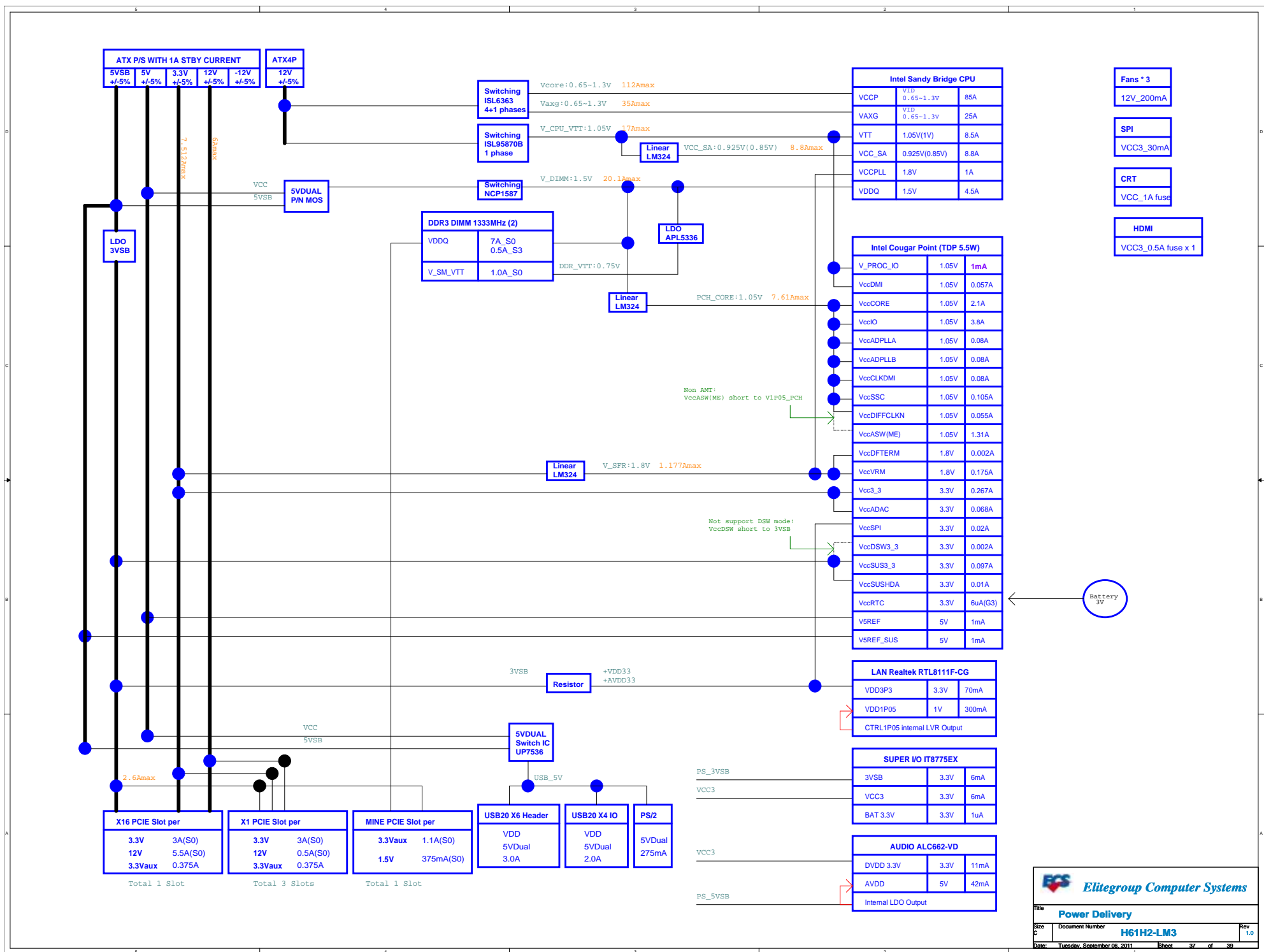
Note:
If 75232 is connected, please use 680 ohm to be the pull down resistor value. Since powered by 12V, 75232 has a very strong internal pull-up. It is hard to be pulled low. (Please see specification for detail of power on strapping setting)

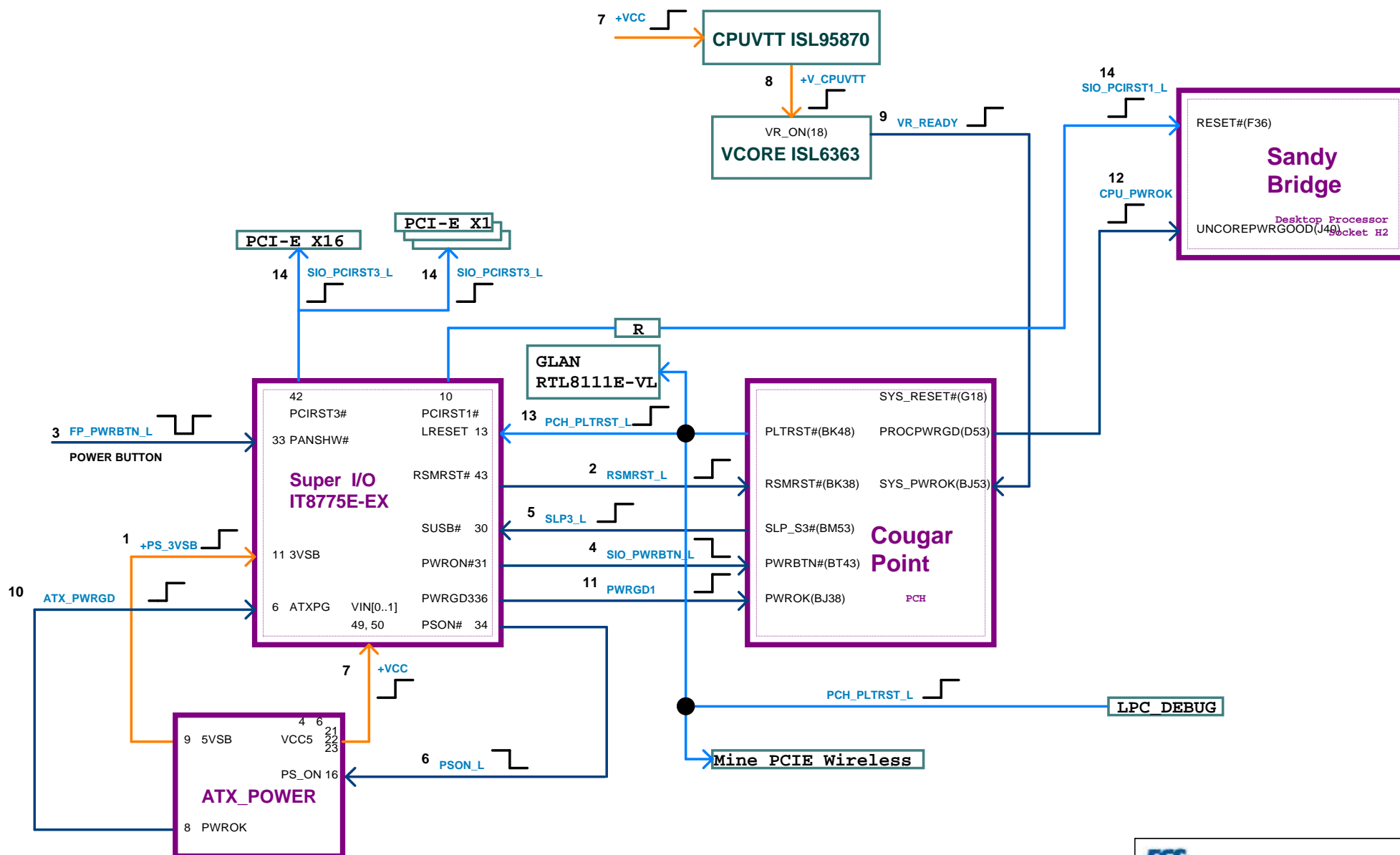


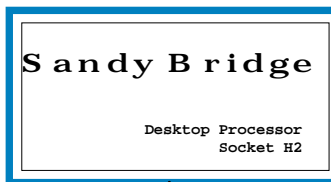
Impedance Test Header



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CK_DIMM_A_[3:0]_H/L

DDR3 Channel A

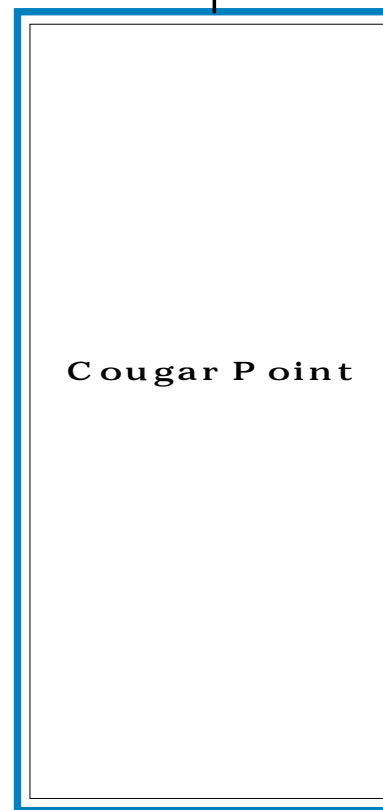
DDR3

1333MHz/1066MHz

CK_DIMM_B_[3:0]_H/L

DDR3 Channel B

CK_CPU_100M_P/N



PEX16_100M_P/N

PCI-E X16

PEX1[A..C]_100M_P/N

PCI-E X1

WLAN_CLK_P/N

Mini PCIE Wireless

GLAN_CLK_P/N

LAN
RTL8111E-VL

XTL 25M

PCI_33M_FB

LDG33M

LPC_DEBUG

SIO33M

SIO:
IT8775E-EX

SIO48M

XTL 32.768K

XTL 25M



Elitegroup Computer Systems

Title
Clock Distribution

Size Custom Document Number
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1.0

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